1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
10		643852	ENGINEERING RELEASED	10/30/08	?

SCHEMATIC,GINSU_A(K50)

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19	20	MCP SATA & USB	K50	10/30/2008
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Preliminary

LAST_MODIFIED=Thu Oct 30 17:51:22 2008

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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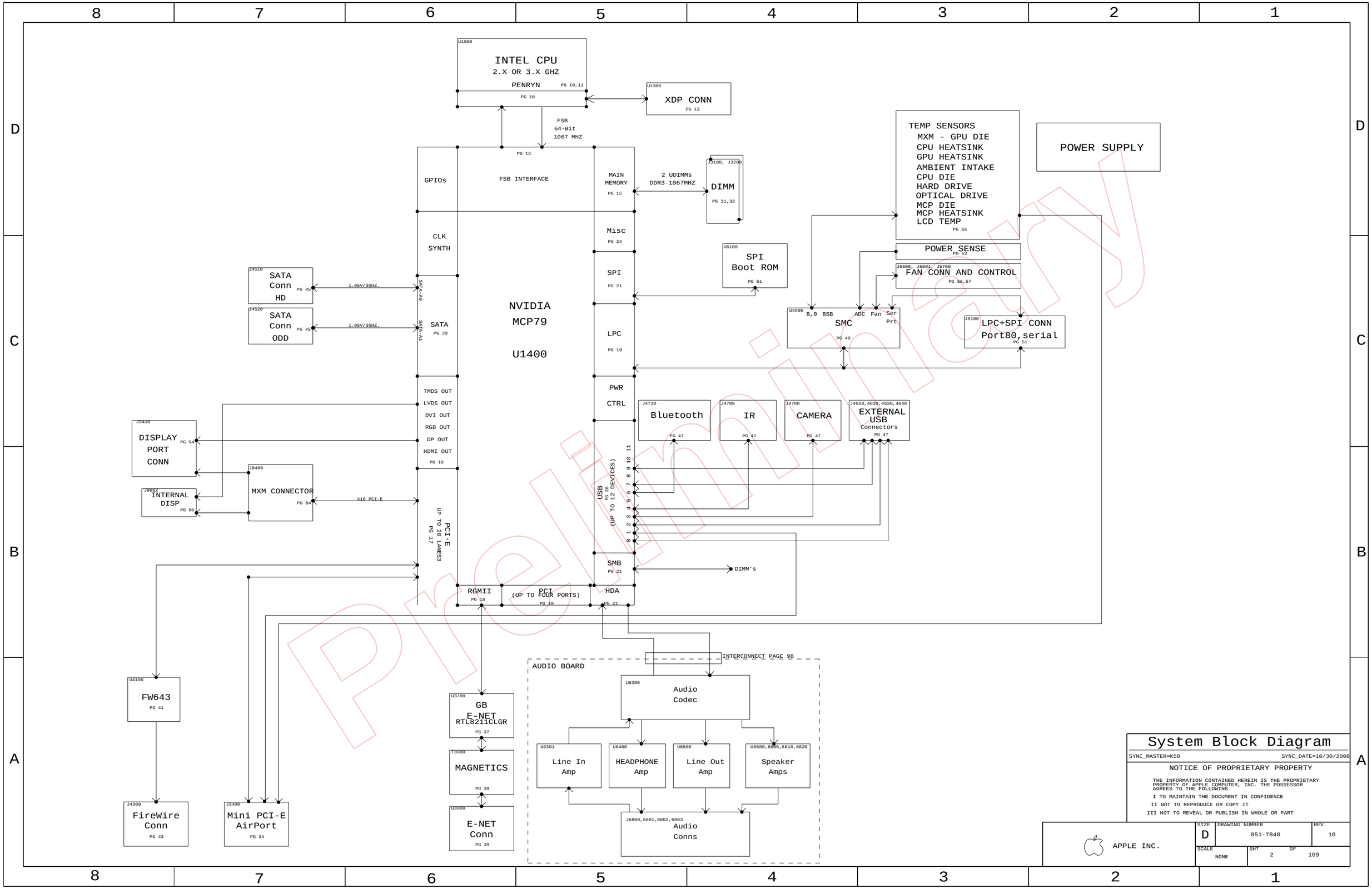
TITLE
SCH,K50,MLB

DRAWING NUMBER 051-7840
REV. 10

DRAWING
SHT 1 OF 109

DRAWING
TITLE=K51
ABBREV=DRAWING
LAST_MODIFIED=Thu Oct 30 17:51:22 2008



System Block Diagram

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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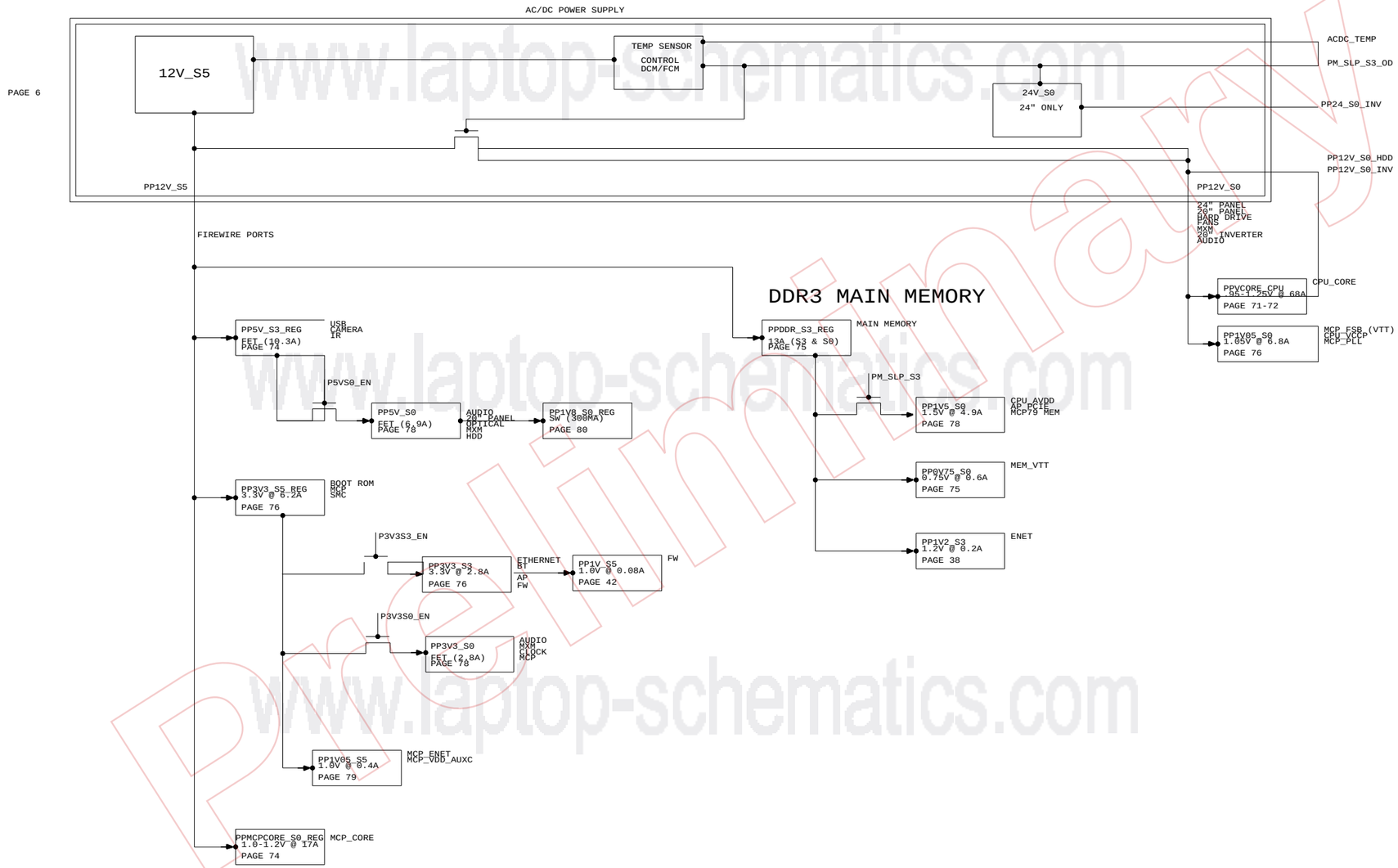
Preliminary



Power Block Diagram

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9501	PCBA,MLB,K50,GOOD	20_INCH_LCD,2P66GHZ_CPU,BASIC,IG
630-9500	PCBA,MLB,K50,CTO	20_INCH_LCD,2P66GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,K50_BETTER,12V_PWR_SENSE
607-2695	K50 MLB DEVELOPMENT	DEVELOPMENT,XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP_TDIODE,MCP79,CPUV_PHASE3,XDP,CPU_TDIODE,MCP_B02
MCP79	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3698	1	IC,PDC,QJTC,QS,2.66,55W,1066,E0,6M,PGA	CPU	CRITICAL	2P66GHZ_CPU
337S3699	1	IC,PDC,QJEX,QS,2.8,55W,1066,E0,6M,PGA	CPU	CRITICAL	2P8GHZ_CPU
337S3700	1	IC,PDC,QJTF,QS,2.93,55W,1066,E0,6M,PGA	CPU	CRITICAL	2P93GHZ_CPU
337S3701	1	IC,PDC,QJTJ,QS,3.06,55W,1066,E0,6M,PGA	CPU	CRITICAL	3P06GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON (DELETED HDCP ROM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0636	1	IC_GMCP_MCP79-B02,35X35MM, BGA1437, DT	U1400	CRITICAL	MCP_B02
338S0654	1	IC,FW643-06,1394B, REV-E	U4100	CRITICAL	
820-2404	1	PCB,FAB,IO ALIGNMENT,K50/K51	IO1	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
341T0135	1	EFI ROM,K50/K51	U6100	CRITICAL	
511S0038	1	CONN,INTEL SKT-P, BGA,26X26-479	U1000	CRITICAL	
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	

K50 PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7577	1	PCB,SCHEM,MLB,K50	SCH1		20_INCH_LCD
	820-2347	1	PCB,FAB,MLB,K50,HF	MLB1		20_INCH_LCD
(338S0563 - BLNK)	341T0132	1	IC,SMC,K50	U4900	CRITICAL	20_INCH_LCD
	114S0305	1	RES,7.87K,0402,1%,1/16W,LF	R7117		20_INCH_LCD
	132S0205	1	CAP,CER,270PF,10%,50V,0402	C7113		20_INCH_LCD
	132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		20_INCH_LCD
	132S0082	1	CAP,CER,0.068UF,10%,10V,0402	C7134		20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
516S0657	988-2127		J3100,J3200	CONN,RCPT,SO-DIMM,DDR3,R/A,204P,LF (NON-HF)

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BOM Configuration

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

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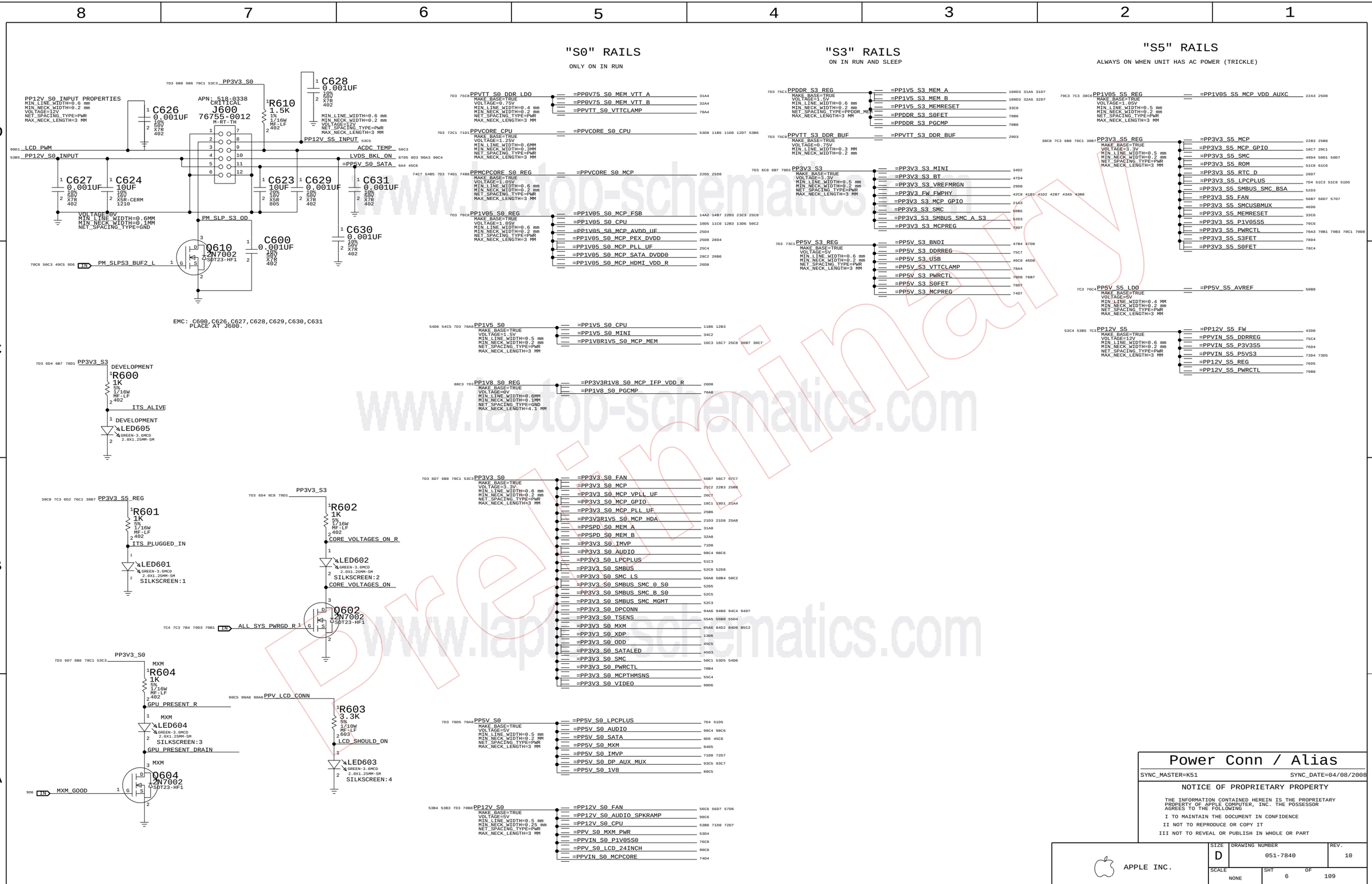

Power Conn / Alias

SYNC_MASTER=K51 SYNC_DATE=04/08/2008

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D	051-7840	10
SCALE NONE	SHT 6 OF 109	

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

100C3 14D6 10D8 7D7	FSB_A_L<6>	PP1000	OMIT P4MM
100C3 14B6 10D8 7D7	FSB_ADSTB_L<0>	PP1001	OMIT P4MM
100C3 14C6 10C8 7D7	FSB_A_L<27>	PP1002	OMIT P4MM
100C3 14B6 10C8 7D7	FSB_ADSTB_L<1>	PP1003	OMIT P4MM
100D3 14D3 10C4 7D7	FSB_D_L<0>	PP1004	OMIT P4MM
100D3 14D6 10C4 7D7	FSB_DSTB_L_P<0>	PP1006	OMIT P4MM
100D3 14D6 10C4 7D7	FSB_DINV_L<0>	PP1007	OMIT P4MM
100D3 14D3 10C4 7D7	FSB_D_L<16>	PP1008	OMIT P4MM
100D3 14D6 10B4 7D7	FSB_DSTB_L_P<1>	PP1010	OMIT P4MM
100D3 14C3 10C2 7D7	FSB_D_L<41>	PP1012	OMIT P4MM
100D3 14D6 10C2 7D7	FSB_DSTB_L_N<2>	PP1013	OMIT P4MM
100D3 14D6 10C2 7D7	FSB_DINV_L<2>	PP1015	OMIT P4MM
100D3 14B3 10B2 7D7	FSB_D_L<59>	PP1016	OMIT P4MM
100D3 14D6 10B2 7D7	FSB_DSTB_L_N<3>	PP1017	OMIT P4MM
100D3 14D6 10B2 7D7	FSB_DINV_L<3>	PP1019	OMIT P4MM
10D6 100B3 14A3	CPU_INIT_L	PP1022	OMIT P4MM
10C8 100C3 14A3	CPU_A20M_L	PP1023	OMIT P4MM
10C8 100B3 14A3	CPU_IGNNE_L	PP1024	OMIT P4MM
10C8 100B3 14A3	CPU_STPCLK_L	PP1025	OMIT P4MM
10C8 100B3 14A3	CPU_INTR	PP1026	OMIT P4MM
10B8 100B3 14A3	CPU_NMI	PP1027	OMIT P4MM
10B8 100B3 14A3	CPU_SMI_L	PP1028	OMIT P4MM
100C3 14B6 10D8 7C7	FSB_REQ_L<0>	PP1029	OMIT P4MM
100C3 14B6 10D8 7C7	FSB_REQ_L<1>	PP1030	OMIT P4MM
100C3 14B6 10D8 7C7	FSB_REQ_L<2>	PP1031	OMIT P4MM
100C3 14B6 10D8 7C7	FSB_REQ_L<3>	PP1032	OMIT P4MM
100C3 14B6 10D8 7C7	FSB_REQ_L<4>	PP1033	OMIT P4MM
10B6 100B3 14B3	FSB_CLK_CPU_P	PP1034	OMIT P4MM
10B6 7B3 100B3 14B3	FSB_CLK_CPU_N	PP1035	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1400

100C3 14D6 10D8 7D8	FSB_A_L<6>	PP1400	OMIT P4MM
100C3 14B6 10D8 7D8	FSB_ADSTB_L<0>	PP1401	OMIT P4MM
100C3 14C6 10C8 7D8	FSB_A_L<27>	PP1402	OMIT P4MM
100C3 14B6 10C8 7D8	FSB_ADSTB_L<1>	PP1403	OMIT P4MM
100D3 14D3 10C4 7D8	FSB_D_L<0>	PP1404	OMIT P4MM
100D3 14D6 10C4 7D8	FSB_DSTB_L_P<0>	PP1406	OMIT P4MM
100D3 14D6 10C4 7D8	FSB_DINV_L<0>	PP1407	OMIT P4MM
100D3 14D3 10C4 7D8	FSB_D_L<16>	PP1408	OMIT P4MM
100D3 14D6 10B4 7D8	FSB_DSTB_L_P<1>	PP1410	OMIT P4MM
100D3 14C3 10C2 7D8	FSB_D_L<41>	PP1412	OMIT P4MM
100D3 14D6 10C2 7D8	FSB_DSTB_L_N<2>	PP1413	OMIT P4MM
100D3 14D6 10C2 7D8	FSB_DINV_L<2>	PP1415	OMIT P4MM
100D3 14B3 10B2 7D8	FSB_D_L<59>	PP1416	OMIT P4MM
100D3 14D6 10B2 7D8	FSB_DSTB_L_N<3>	PP1417	OMIT P4MM
100D3 14D6 10B2 7D8	FSB_DINV_L<3>	PP1419	OMIT P4MM
14B6 100C3 10D6	FSB_LOCK_L	PP1420	OMIT P4MM
100C3 14B6 10D6	FSB_HIT_L	PP1421	OMIT P4MM
100C3 14B6 10D6	FSB_HITM_L	PP1422	OMIT P4MM
100C3 14B6 10D6	FSB_BNR_L	PP1423	OMIT P4MM
100C3 23C3 14B6 10D6	FSB_BREQ0_L	PP1424	OMIT P4MM
100C3 14B6 10D6	FSB_DBSY_L	PP1425	OMIT P4MM
10B2 100B3 14A3	FSB_DPWR_L	PP1426	OMIT P4MM
100C3 14B6 10D8 7C8	FSB_REQ_L<0>	PP1427	OMIT P4MM
100C3 14B6 10D8 7C8	FSB_REQ_L<1>	PP1428	OMIT P4MM
100C3 14B6 10D8 7C8	FSB_REQ_L<2>	PP1429	OMIT P4MM
100C3 14B6 10D8 7C8	FSB_REQ_L<3>	PP1430	OMIT P4MM
100C3 14B6 10D8 7C8	FSB_REQ_L<4>	PP1431	OMIT P4MM
70A3 7C4 71C7	VR_PWRGOOD_DELAY	PP1434	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U3700

37B7 18C3	ENET_RESET_L	PP3704	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4100

41C2 102C3 17C3	PCIE_CLK100M_FW_P	PP4000	OMIT P4MM
41C2 102C3 17C3	PCIE_CLK100M_FW_N	PP4001	OMIT P4MM
41C3 102D3	PCIE_FW_R2D_P	PP4002	OMIT P4MM
41C3 102D3	PCIE_FW_R2D_N	PP4003	OMIT P4MM
41A2 7B3 9C2	FW_RESET_L	PP4004	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4900

49C8 9D2	SMC_LRESET_L	PP4901	OMIT P4MM
49C3 7D4 51C4 50D6	SMC_RESET_L	PP4902	OMIT P4MM
7D4 103D3 51D5 49C8 19B3 7B8	LPC_AD<1>	PP4903	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1400

17B6 102D3 34C8	PCIE_MINI_D2R_P	PP2105	OMIT P4MM
17B6 102D3 34C8	PCIE_MINI_D2R_N	PP2106	OMIT P4MM
17B6 102C3 41C1	PCIE_FW_D2R_P	PP2132	OMIT P4MM
17B6 102C3 41C1	PCIE_FW_D2R_N	PP2133	OMIT P4MM
28B8 7C3 49B8	PM_SYSRST_L	PP2113	OMIT P4MM
19B7 7D4 51D5 49C5	PM_CLKRUN_L	PP2114	OMIT P4MM
20D6 102B3 45C5	SATA_ODD_D2R_P	PP4904	OMIT P4MM
20D6 102B3 45C5	SATA_ODD_D2R_N	PP4905	OMIT P4MM
20D6 102C3 45C5	SATA_HDD_D2R_P	PP2119	OMIT P4MM
20D6 102C3 45D5	SATA_HDD_D2R_N	PP2120	OMIT P4MM
51D5 49C8 19B3 7D6 7D4 103D3	LPC_AD<1>	PP2121	OMIT P4MM
103C3 47B7 20D3	USB_CAMERA_P	PP2122	OMIT P4MM
103C3 47B7 20D3	USB_CAMERA_N	PP2123	OMIT P4MM
47D4 103C3 20D3	USB_BT_P	PP2126	OMIT P4MM
47D4 103C3 20C3	USB_BT_N	PP2127	OMIT P4MM
61C6 51A6 103B3 21B3	SPI_CLK_R	PP2128	OMIT P4MM
21B3 103B3 61B2 51A6	SPI_MISO	PP2129	OMIT P4MM

101D3 31C4 15B7	MEM_A_DQ<7>	PP1442	OMIT P4MM
101D3 31C2 15B7	MEM_A_DQ<14>	PP1443	OMIT P4MM
101D3 31B4 15B7	MEM_A_DQ<16>	PP1444	OMIT P4MM
101D3 31C4 15C7	MEM_A_DQ<25>	PP1445	OMIT P4MM
101C3 31B7 15D7	MEM_A_DQ<47>	PP1447	OMIT P4MM
101C3 31A7 15D7	MEM_A_DQ<59>	PP1449	OMIT P4MM
101C3 31C4 15D5	MEM_A_DQS_P<1>	PP1452	OMIT P4MM
101C3 31B2 15D5	MEM_A_DQS_P<2>	PP1454	OMIT P4MM
101C3 31C4 15D5	MEM_A_DQS_P<3>	PP1456	OMIT P4MM
101C3 31B7 15D5	MEM_A_DQS_P<4>	PP1458	OMIT P4MM
101C3 31B5 15D5	MEM_A_DQS_P<5>	PP1460	OMIT P4MM
101B3 31B7 15D5	MEM_A_DQS_N<6>	PP1463	OMIT P4MM
101B3 32C4 15B3	MEM_B_DQ<6>	PP1466	OMIT P4MM
101B3 32C4 15B3	MEM_B_DQ<8>	PP1467	OMIT P4MM
101B3 32B4 15C3	MEM_B_DQ<23>	PP1468	OMIT P4MM
101B3 32C4 15C3	MEM_B_DQ<25>	PP1469	OMIT P4MM
101A3 32B7 15C3	MEM_B_DQ<38>	PP1470	OMIT P4MM
101A3 32A5 15D3	MEM_B_DQ<62>	PP1473	OMIT P4MM
101D1 32B2 15D1	MEM_B_DQS_P<2>	PP1478	OMIT P4MM
101D1 32C4 15D1	MEM_B_DQS_N<3>	PP1481	OMIT P4MM
101D1 32B7 15D1	MEM_B_DQS_N<4>	PP1483	OMIT P4MM
101D1 32B5 15D1	MEM_B_DQS_P<5>	PP1484	OMIT P4MM
101D1 32B5 15D1	MEM_B_DQS_N<5>	PP1485	OMIT P4MM
101D1 32B7 15D1	MEM_B_DQS_P<6>	PP1486	OMIT P4MM
101D1 32A5 15D1	MEM_B_DQS_N<7>	PP1489	OMIT P4MM
9C6 102D3 86C1	PEG_D2R_P<7>	PP1490	OMIT P4MM
9C6 102D3 86C1	PEG_D2R_N<7>	PP1491	OMIT P4MM

LPC CONNECTOR

51D5 51C8 51C3 6D1	IN	=PP3V3_S5_LPCPLUS	FUNC_TEST=TRUE
51D5 6A4	IN	=PP5V_S0_LPCPLUS	FUNC_TEST=TRUE
51D4 103D3 9B2	IN	LPC_CLK33M_LPCPLUS	FUNC_TEST=TRUE
103D3 51D5 49C8 19B3	IN	LPC_AD<0>	FUNC_TEST=TRUE
103D3 51D5 49C8 19B3 7D6 7B8	IN	LPC_AD<1>	FUNC_TEST=TRUE
103D3 51D4 49C8 19B3	IN	LPC_AD<2>	FUNC_TEST=TRUE
103D3 51D4 49C8 19B3	IN	LPC_AD<3>	FUNC_TEST=TRUE
51D5 49C8 103D3 19C3	IN	LPC_FRAME_L	FUNC_TEST=TRUE
19B7 51D5 49C5 7C8	IN	PM_CLKRUN_L	FUNC_TEST=TRUE
50D3 49B5 51D5	IN	SMC_TMS	FUNC_TEST=TRUE
51D5 9D2	IN	DEBUG_RESET_L	FUNC_TEST=TRUE
51C5 49C1	IN	SMC_TRST_L	FUNC_TEST=TRUE
50D3 51D5 49B5	IN	SMC_TDO	FUNC_TEST=TRUE
49C1 51C5	IN	SMC_MD1	FUNC_TEST=TRUE
51C5 50D3 49C5 49B8 46D5	IN	SMC_TX_L	FUNC_TEST=TRUE
51D4 49C8 19B7	IN	LPC_SERIRQ	FUNC_TEST=TRUE
50D3 49B5 51D4	IN	SMC_TDI	FUNC_TEST=TRUE
50D3 49B5 51D4	IN	SMC_TCK	FUNC_TEST=TRUE
49C3 51C4 50D6 7D6	IN	SMC_RESET_L	FUNC_TEST=TRUE
49C1 51C4	IN	SMC_NMI	FUNC_TEST=TRUE
50D3 49C5 49B8 51C4 46D5	IN	SMC_RX_L	FUNC_TEST=TRUE
51D4 49C5 19C3	IN	LPC_PWRDWN_L	FUNC_TEST=TRUE
51C4 18B7	IN	LPCPLUS_GPIO	FUNC_TEST=TRUE
51D4 51A8	IN	SPI_ALT_CLK	FUNC_TEST=TRUE
51D4 51C8	IN	SPI_ALT_CS_L	FUNC_TEST=TRUE
51D5 51A8	IN	SPI_ALT_MOSI	FUNC_TEST=TRUE
51A8 51D5	IN	SPI_ALT_MISO	FUNC_TEST=TRUE
51D4 51C7	IN	SPIROM_USE_MLB	FUNC_TEST=TRUE
		GND 16 TP'S	FUNC_TEST=TRUE
			MIN_ALLOWED_TPS=16

PWROK SEQUENCING

7C3 7B4 6B7 78D3 70B1	IN	ALL_SYS_PWRGD_R	FUNC_TEST=TRUE

STARTUP (BOOT/WAKE) TIMING

71C7 49D8	IN	IMVP_VR_ON	FUNC_TEST=TRUE
70A3 71C7 7C7	IN	VR_PWRGOOD_DELAY	FUNC_TEST=TRUE

SHUTDOWN/SLEEP TIMING

9D7 102B3 21C3	IN	PM_SLP_S3_L	FUNC_TEST=TRUE
70D8 50C3 49C5 38D7 102B3 21C3	IN	PM_SLP_S4_L	FUNC_TEST=TRUE
7C4 7C3 6B7 70D3 70B1	IN	ALL_SYS_PWRGD_R	FUNC_TEST=TRUE
13C7 10B2 100B3 14A3	IN	CPU_PWRGD	FUNC_TEST=TRUE

XDP CONNECTOR

100A3 13C6 10C6 10C5	IN	XDP_BPM_L<5..0>	FUNC_TEST=TRUE
13C6	IN	TP_XDP_OBSFN_B0	FUNC_TEST=TRUE
13C6	IN	TP_XDP_OBSFN_B1	FUNC_TEST=TRUE
13C6	IN	TP_XDP_OBSDATA_B0	FUNC_TEST=TRUE
13C6	IN	TP_XDP_OBSDATA_B1	FUNC_TEST=TRUE
13C6	IN	TP_XDP_OBSDATA_B2	FUNC_TEST=TRUE
13C6	IN	TP_XDP_OBSDATA_B3	FUNC_TEST=TRUE
13C6	IN	XDP_PWRGD	FUNC_TEST=TRUE
13C6 19C4	IN	PM_LATRIGGER_L	FUNC_TEST=TRUE
52D8 106D3 21C3 13B6	IN	SMBUS_MCP_0_DATA	FUNC_TEST=TRUE
52D8 106D3 21C3 13B6	IN	SMBUS_MCP_0_CLK	FUNC_TEST=TRUE
19D7 13C3	IN	MCP_DEBUG<0..7>	FUNC_TEST=TRUE
13C3 100B3 14B3	IN	FSB_CLK_ITP_P	FUNC_TEST=TRUE
13C3 100B3 14B3	IN	FSB_CLK_ITP_N	FUNC_TEST=TRUE
13C4 100A3	IN	XDP_CPURST_L	FUNC_TEST=TRUE
28B8 13B3 10C6	IN	XDP_DBRESET_L	FUNC_TEST=TRUE
10C6 10A6 100A3 13B3	IN	XDP_TRST_L	FUNC_TEST=TRUE
10C6 10B6 100A3 13B3	IN	XDP_TDI	FUNC_TEST=TRUE
10C6 10B6 100A3 13B3	IN	XDP_TMS	FUNC_TEST=TRUE
13B3 10B6 100A3 10C6	IN	XDP_TDO	FUNC_TEST=TRUE
10C6 10A6 100A3 13B6	IN	XDP_TCK	FUNC_TEST=TRUE
21B7 13C3	IN	JTAG_MCP_TDI	FUNC_TEST=TRUE
21B7 13C3	IN	JTAG_MCP_TMS	FUNC_TEST=TRUE
21B7 13B6	IN	JTAG_MCP_TCK	FUNC_TEST=TRUE
13C3 21B7	IN	JTAG_MCP_TDO	FUNC_TEST=TRUE
21B7 13C3	IN	JTAG_MCP_TRST_L	FUNC_TEST=TRUE

"S0" RAILS

10 TP'S

6D6 75C8	IN	PPVTT_S0_DDR_LDO	FUNC_TEST=TRUE
6D6 72C1 71D1	IN	PPVCORE_CPU	FUNC_TEST=TRUE
74C7 54B5 6D6 74D1 74B8	IN	PPMCPCORE_S0_REG	FUNC_TEST=TRUE
6D6 76C8	IN	PP1V05_S0_REG	FUNC_TEST=TRUE
54D6 54C5 6C6 70A8	IN	PP1V5_S0	FUNC_TEST=TRUE
80C3 6C6	IN	PP1V8_S0_REG	FUNC_TEST=TRUE
6D7 6B8 6B6 78C1 53C3	IN	PP3V3_S0	FUNC_TEST=TRUE
6A6 78D5 70A8	IN	PP5V_S0	FUNC_TEST=TRUE
53B4 53B3 6A6 70B8	IN	PP12V_S0	FUNC_TEST=TRUE

"S3" RAILS

4 TP'S

6D4 75C1	IN	PPDDR_S3_REG	FUNC_TEST=TRUE
6D4 75C8	IN	PPVTT_S3_DDR_BUF	FUNC_TEST=TRUE
6D4 6C8 6B7 78D1	IN	PP3V3_S3	FUNC_TEST=TRUE
6C4 73C1	IN	PP5V_S3_REG	FUNC_TEST=TRUE

"S5" RAILS

3 TP'S

79C3 6D2 38C6	IN	PP1V05_S5_REG	FUNC_TEST=TRUE
38C8 6D2 6B8 76C1 38B7	IN	PP3V3_S5_REG	FUNC_TEST=TRUE
6C2 76C4	IN	PP5V_S5_LDO	FUNC_TEST=TRUE
53C4 53B5 6C2	IN	PP12V_S5	FUNC_TEST=TRUE

28B8 49B8 7C8	IN	PM_SYSRST_L	FUNC_TEST=TRUE
50D7	IN	SMC_MANUAL_RST_L	FUNC_TEST=TRUE
7C4 7B4 6B7 78D3 70B1	IN	ALL_SYS_PWRGD_R	FUNC_TEST=TRUE

FOR ICT

102C3 87C5 9C6	IN	GPU_CLK100M_PCIE_N	FUNC_TEST=TRUE
10B6 100B3 14B3 7C8	IN	FSB_CLK_CPU_N	FUNC_TEST=TRUE
19D7 19D2 103D3	IN	PCI_REQ0_L	FUNC_TEST=TRUE
19D7 19D2 103D3	IN	PCI_REQ1_L	FUNC_TEST=TRUE
41B2	IN	TP_FW643_TCK	FUNC_TEST=TRUE
41B2	IN	TP_FW643_TMS	FUNC_TEST=TRUE
41B2	IN	TP_FW643_TDI	FUNC_TEST=TRUE
41B2	IN	TP_FW643_TDO	FUNC_TEST=TRUE
41B6	IN	TP_FW643_SM	FUNC_TEST=TRUE
41B6	IN	TP_FW643_SE	FUNC_TEST=TRUE
41B6	IN	TP_FW643_NAND_TREE	FUNC_TEST=TRUE
41A6	IN	TP_FW643_CE	FUNC_TEST=TRUE
41A2 9C2 7D6	IN	FW_RESET_L	FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA, ZH510 HOLE-VIA, ZH520 HOLE-VIA
ZH501 HOLE-VIA, ZH511 HOLE-VIA, ZH521 HOLE-VIA
ZH502 HOLE-VIA, ZH512 HOLE-VIA, ZH522 HOLE-VIA
ZH503 HOLE-VIA, ZH513 HOLE-VIA, ZH523 HOLE-VIA
ZH504 HOLE-VIA, ZH514 HOLE-VIA, ZH524 HOLE-VIA
ZH505 HOLE-VIA, ZH515 HOLE-VIA, ZH525 HOLE-VIA
ZH506 HOLE-VIA, ZH516 HOLE-VIA, ZH526 HOLE-VIA
ZH507 HOLE-VIA, ZH517 HOLE-VIA, ZH527 HOLE-VIA
ZH508 HOLE-VIA, ZH518 HOLE-VIA, ZH528 HOLE-VIA
ZH509 HOLE-VIA, ZH519 HOLE-VIA, ZH529 HOLE-VIA

ZH536 HOLE-VIA
ZH531 HOLE-VIA, ZH534 HOLE-VIA, ZH537 HOLE-VIA
ZH532 HOLE-VIA, ZH535 HOLE-VIA

CRITICAL
SC0700 EMI-SPRING CLIP-SM1
SC0701 EMI-SPRING CLIP-SM1
CRITICAL BTW DIMMS
SC0702 EMI-SPRING CLIP-SM-K2

835-0266
CRITICAL SDF0726 NUT-6.5OD1.8H-1.56-3.8-TH
CRITICAL SDF0727 NUT-6.5OD1.8H-1.56-3.8-TH

998-0846 FOR MCP HEATSINK
OMIT ZH0722 4R3P25, OMIT ZH0723 4R3P25, OMIT ZH0725 4R3P25, OMIT ZH0730 4R3P25

998-0850
OMIT ZH0700 4P75R4, OMIT ZH0701 4P75R4, OMIT ZH0702 4P75R4, OMIT ZH0703 4P75R4

998-0847
OMIT ZH0711 5R3P5-6B 998-1608, OMIT ZH0712 4P25R3P5, OMIT ZH0713 4P25R3P5, OMIT ZH0714 4P25R3P5, OMIT ZH0715 4P25R3P5

CRITICAL 860-0895 SDF0717 STDOFF-7P0OD15P0H-TH

998-0847
OMIT ZH0718 4P25R3P5, OMIT ZH0720 4P25R3P5

Functional / ICT Test

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10
SCALE NONE	SHT 7 OF 109	

Preliminary
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NC ON UNUSED ALIASES

18C6	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE NO_TEST=TRUE
18C6	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE NO_TEST=TRUE
18C6	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE NO_TEST=TRUE
18C6	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	TP_MCP_RGB_HSYNC	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	TP_MCP_RGB_VSYNC	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19C7	TP_PCI_AD<31..15>	NC_PCI_AD<31..15>	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_C_BE_L<1..0>	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19B7	TP_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE
21B3	TP_MCP_BUF_SIO_CLK	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_ODT<3..2>	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE NO_TEST=TRUE
16D6 16C6	TP_MEM_A_CKE<3..2>	NC_MEM_A_CKE<3..2>	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CS_L<3..2>	NC_MEM_A_CS_L<3..2>	MAKE_BASE=TRUE NO_TEST=TRUE
15B5	TP_MEM_A_CLK2P	NC_MEM_A_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15B5	TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CLK3P	NC_MEM_A_CLK3P	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CLK3N	NC_MEM_A_CLK3N	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CLK4P	NC_MEM_A_CLK4P	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CLK4N	NC_MEM_A_CLK4N	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CLK5P	NC_MEM_A_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16D6	TP_MEM_A_CLK5N	NC_MEM_A_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CS_L<3..2>	NC_MEM_B_CS_L<3..2>	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_ODT<3..2>	NC_MEM_B_ODT<3..2>	MAKE_BASE=TRUE NO_TEST=TRUE
16D3 16C3	TP_MEM_B_CKE<3..2>	NC_MEM_B_CKE<3..2>	MAKE_BASE=TRUE NO_TEST=TRUE
15B1	TP_MEM_B_CLK2P	NC_MEM_B_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15B1	TP_MEM_B_CLK2N	NC_MEM_B_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CLK3P	NC_MEM_B_CLK3P	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CLK3N	NC_MEM_B_CLK3N	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CLK4P	NC_MEM_B_CLK4P	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CLK4N	NC_MEM_B_CLK4N	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CLK5P	NC_MEM_B_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16D3	TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE

18C6	TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE NO_TEST=TRUE
18C3	TP_ENET_PWRDWN_L	NC_ENET_PWDWN_L	MAKE_BASE=TRUE NO_TEST=TRUE
21C7	TP_MCP_KBDRSTIN_L	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE NO_TEST=TRUE
17B6	TP_MCP_GPIO_18	NC_MCP_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE
23D7	TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_C_BE_L<3>	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE NO_TEST=TRUE
19C4	TP_PCI_CLK0	NC_PCI_CLK0	MAKE_BASE=TRUE NO_TEST=TRUE
19C4	TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_GNT0_L	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19C7	TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE NO_TEST=TRUE
19C7	TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE NO_TEST=TRUE
19C7	TP_PCI_INTY_L	NC_PCI_INTY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19C7	TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
19C4	TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE NO_TEST=TRUE
19C7	TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
17C3	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
17C3	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
17B3	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
17B3	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
17B3	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
17C6	PCIE_EXCARD_PRSNT_L	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
17C6	TP_PE4_CLKREQ_L	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
17C6	TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
21C7	TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE NO_TEST=TRUE
20C3	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20C3	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20C3	TP_USB_11N	NC_USB_11N	MAKE_BASE=TRUE NO_TEST=TRUE
20C3	TP_USB_11P	NC_USB_11P	MAKE_BASE=TRUE NO_TEST=TRUE
20C3	USB_EXCARD_N	NC_USB_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20C3	USB_EXCARD_P	NC_USB_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
21B3	ODD_PWR_EN_L	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE NO_TEST=TRUE
17C3	PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
17C3	PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
17C6	EXCARD_CLKREQ_L	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19D7	TP_PCI_AD<12..10>	NC_PCI_AD<12..10>	MAKE_BASE=TRUE NO_TEST=TRUE
19D7	TP_PCI_AD<8>	NC_PCI_AD<8>	MAKE_BASE=TRUE NO_TEST=TRUE

TESTPOINT ALIAS FOR UNUSED NETS

17B6	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
17B6	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
17B3	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
17B3	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
71C7	VR_PWRGD_CLKEN_L	TP_VR_PWRGD_CLKEN_L	MAKE_BASE=TRUE
90C4 90A3 6D6 87D6	LVDS_BKL_ON	LVDS_BKL_ON	MAKE_BASE=TRUE

UNUSED INTERNAL USB PORTS

20D3	USB_TPAD_N	TP_USB_TPAD_N	MAKE_BASE=TRUE
20D3	USB_TPAD_P	TP_USB_TPAD_P	MAKE_BASE=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

31D5	MEM_A_A<15>	TP_MEM_A_A<15>	MAKE_BASE=TRUE
32D5	MEM_B_A<15>	TP_MEM_B_A<15>	MAKE_BASE=TRUE

TESTPOINT FOR OPTIONAL GMUX JTAG FROM MCP

17B6	GMUX_JTAG_TCK_L	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE NO_TEST=TRUE
17B6	GMUX_JTAG_TDO	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	GMUX_JTAG_TDI	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE NO_TEST=TRUE
19D4	GMUX_JTAG_TMS	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE NO_TEST=TRUE

K51 ONLY STANDOFFS

CRITICAL
860-0895
SDF0800
STDOFF-7P0OD15P0H-TH

CRITICAL
860-0895
SDF0801
STDOFF-7P0OD15P0H-TH

UNUSED SIGNAL ALIAS/STAND OFF

SYNC_MASTER=K51 SYNC_DATE=04/07/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

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SIGNAL ALIAS

10B2 CPU_PSI_L — IMVP6_PSI_L (MAKE_BASE=TRUE) 71C7

21D7 TP_MLB_RAM_VENDOR — MXM_GOOD (MAKE_BASE=TRUE) 6A8

7B4 102B3 21C3 PM_SLP_S3_L — R910 15 (5% 1/16W MF-LF 402) — PM_SLPS3_BUF2_L (MAKE_BASE=TRUE) 6C8 49C5 50C3 70C8

(P50 HAS A 100K TO GROUND)

R911 15 (5% 1/16W MF-LF 402) — PM_SLPS3_BUF1_L (MAKE_BASE=TRUE) 73A6 94D7

R912 100K (5% 1/16W MF-LF 402)

PEG Slot Support

17C3 IN	PEG_CLK100M_P	GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE)	OUT 87C5 102C3
17C3 IN	PEG_CLK100M_N	GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE)	OUT 87C5 102C3 7C3
17D3 17C3 IN	=PEG_R2D_C_P<0..15>	PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE)	OUT 102D3 86A7 86B7 86C7 86D7
17D3 17C3 IN	=PEG_R2D_C_N<0..15>	PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE)	OUT 102D3 86A7 86B7 86C7 86D7
17D6 17C6 OUT	=PEG_D2R_P<0..15>	PEG_D2R_P<0..15> (MAKE_BASE=TRUE)	IN 7B7 86A1 86B1 86C1 86D1 102D3
17D6 17C6 OUT	=PEG_D2R_N<0..15>	PEG_D2R_N<0..15> (MAKE_BASE=TRUE)	IN 7B7 86A1 86B1 86C1 86D1 102D3
17C6 IN	PEG_PRSNT_L	MXM_DETECT_L (MAKE_BASE=TRUE)	OUT 85B6 85B3

DisplayPort / TMDS Support

18B6 IN	=MCP_HDMI_TXC_P	DP_IG_ML_P<3> (MAKE_BASE=TRUE)	OUT 107D2 91C4
18B6 IN	=MCP_HDMI_TXC_N	DP_IG_ML_N<3> (MAKE_BASE=TRUE)	OUT 107D2 91D4
18B6 IN	=MCP_HDMI_TXD_P<0..2>	DP_IG_ML_P<2..0> (MAKE_BASE=TRUE)	OUT 107D2 91B7 91B8 91C8
18B6 IN	=MCP_HDMI_TXD_N<0..2>	DP_IG_ML_N<2..0> (MAKE_BASE=TRUE)	OUT 107D2 91B8 91C8 91D8
18A3 IN	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK (MAKE_BASE=TRUE)	OUT 93C8
18A3 BI	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA (MAKE_BASE=TRUE)	BI 93D8
18B6 OUT	=MCP_HDMI_HPD	DP_IG_HPD (MAKE_BASE=TRUE)	IN 91B4

18B6 =DVI_HPD_GMUX_INT — HPLUG_DET2 (MAKE_BASE=TRUE) — R900 20K (5% 1/16W MF-LF 402)

MCP79 PCIe PRSNT# Straps

PCIE_FW_PRSNT_L — OUT 17C6

PCIE_MINI_PRSNT_L — OUT 17C6

USB ALIAS

70D8 IN PGOOD_5V_S3 — PM_EN_USB_PWR OUT 46C8

GROUND ALIAS

GND RAILS

98D6 GND_AUDIO_SPKRAMP

GND (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.09MM, VOLTAGE=0V, NET_SPACING_TYPE=GND, MAKE_BASE=TRUE, MAX_NECK_LENGTH=4.1 MM)

Platform Reset Connections

LPC Reset (Unbuffered)

103D3 19C3 IN LPC_RESET_L — PLACEMENT_NOTE=Place close to U1400 — R981 33 (5% 1/16W MF-LF 402) — DEBUG_RESET_L OUT 7D4 51D5

PLACEMENT_NOTE=Place close to U1400 — R983 33 (5% 1/16W MF-LF 402) — SMC_LRESET_L OUT 7D6 49C8

PCIE Reset (Unbuffered)

17B3 IN PCIE_RESET_L

R992 0 (5% 1/16W MF-LF 402) — FW_RESET_L OUT 7D6 7B3 41A2

R991 0 (5% 1/16W MF-LF 402) — MINI_RESET_L OUT 34C3

R990 0 (5% 1/16W MF-LF 402) — PEG_RESET_L OUT 87C5 90D4

R971 0 (5% 1/16W MF-LF 402) — PCA9557D_RESET_L OUT 29A5

19C4 IN MEM_VTT_EN_R — R972 33 (5% 1/16W MF-LF 402) — DDRVTT_EN OUT 75C8 78A4

NO STUFF C973 0.47UF (10% 6.3V CERM-X5R 402)

103D3 19B3 IN LPC_CLK33M_SMC_R — PLACEMENT_NOTE=Place close to U1400 — R925 33 (5% 1/16W MF-LF 402) — LPC_CLK33M_SMC OUT 103D3 49C8

PLACEMENT_NOTE=Place close to U1400 — R926 33 (5% 1/16W MF-LF 402) — LPC_CLK33M_LPCPLUS OUT 103D3 7D4 51D4

103D3 21B3 IN PM_CLK32K_SUSCLK_R — PLACEMENT_NOTE=Place close to U1400 — R929 22 (5% 1/16W MF-LF 402) — PM_CLK32K_SUSCLK OUT 103D3 49C5

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

21B3 IN MCP_CPUVDD_EN — PLACEMENT_NOTE=Place close to U1400 — R930 22 (5% 1/16W MF-LF 402) — MCP_CPU_VLD OUT 21B7

18D6 =MCP_MII_RXER
18D6 =MCP_MII_COL
18D6 =MCP_MII_CRS

MCP_MII_NU (MAKE_BASE=TRUE) — R955 47K (5% 1/16W MF-LF 402)

SIGNAL & GND ALIASES	
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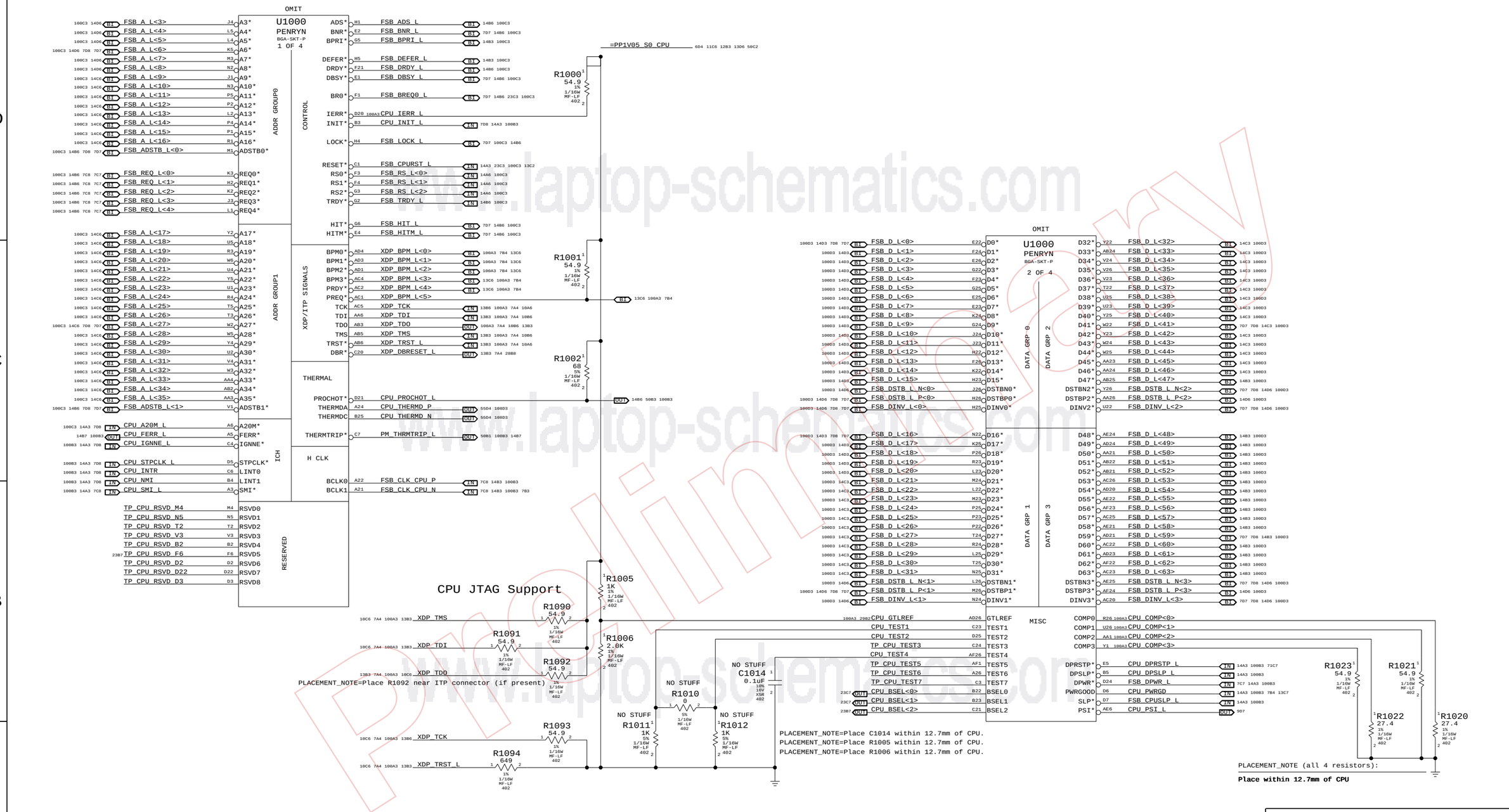

CPU FSB

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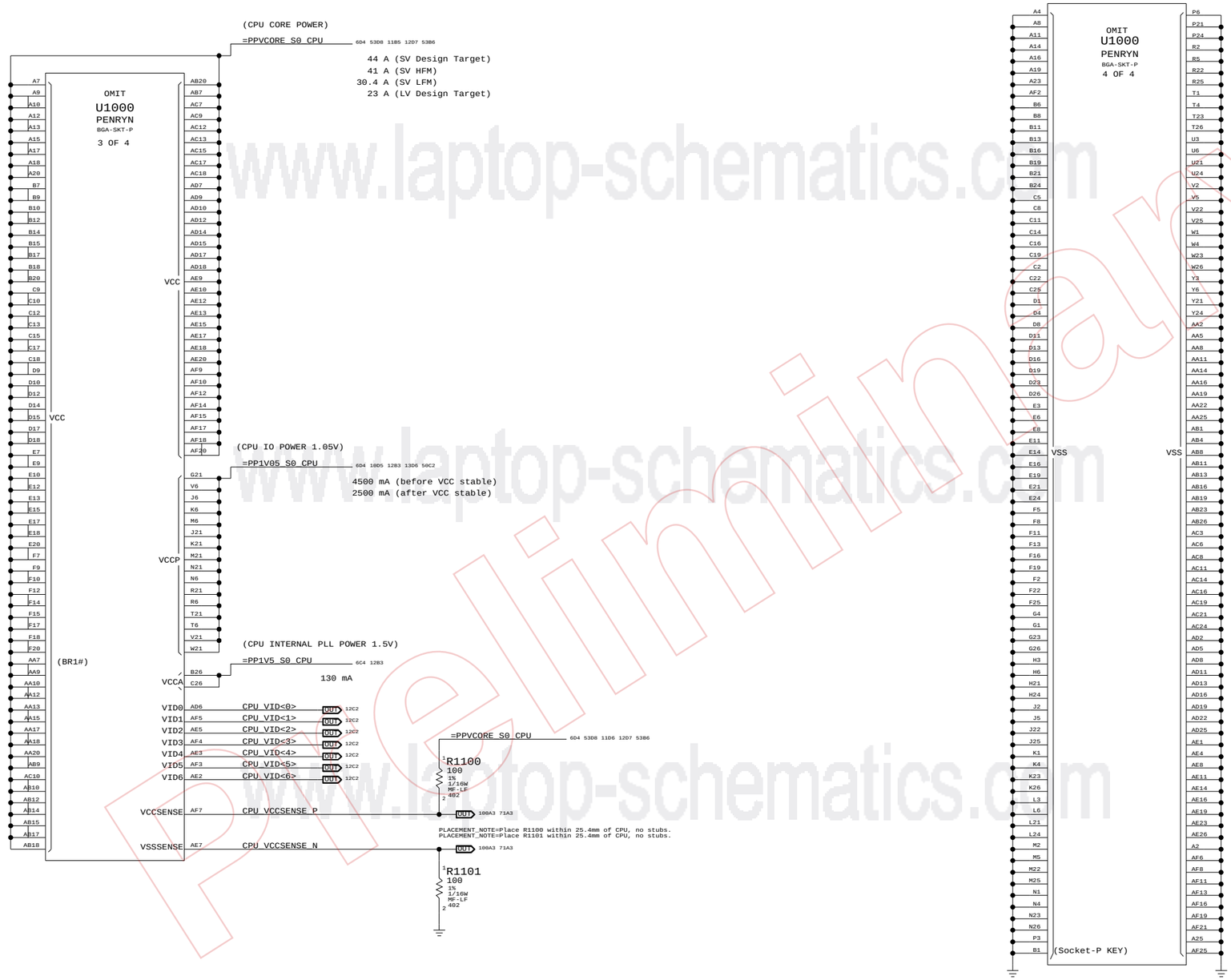

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

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CPU VCORE HF AND BULK DECOUPLING

6X 220UF. 32X 22UF 0805

53B6 11D6 11B5 53D8 6D4 =PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

NOSTUFF C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209
22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1210, C1211, C1212, C1213, C1214, C1215, C1216, C1217, C1218, C1219
22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)

C1220, C1221, NOSTUFF C1222, NOSTUFF C1223, NOSTUFF C1224, NOSTUFF C1225
22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

C1226, C1227, NOSTUFF C1228, NOSTUFF C1229, C1230, NOSTUFF C1231
22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CRITICAL NOSTUFF C1250, CRITICAL C1251, CRITICAL C1254, CRITICAL C1255, CRITICAL C1252, CRITICAL C1253
220UF-0.007OHM 20% 2V POLY CASE-D2-SM

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

LAYOUT NOTE:
PLACE NEAR MCP

C1260, C1261, C1262, C1263, C1264, C1265
0.1UF 20% 10V CERM 402

CPU VCORE VID CONNECTIONS

11B6 CPU_VID<0> — IMVP6_VID<0> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<1> — IMVP6_VID<1> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<2> — IMVP6_VID<2> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<3> — IMVP6_VID<3> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<4> — IMVP6_VID<4> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<5> — IMVP6_VID<5> MAKE_BASE=TRUE 100A3 71C7
11B6 CPU_VID<6> — IMVP6_VID<6> MAKE_BASE=TRUE 100A3 71C7

VCCA (CPU AVdd) DECOUPLING

11B6 6C4 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603

C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

50C2 13D6 11C6 10D5 6D4 =PP1V05_S0_CPU

1X 330UF, 6X 0.1UF 0402

CRITICAL C1235 330UF 20% 6.3V ELEC 6.3X8-SM-HF

C1236, C1237, C1238, C1239, C1240, C1241
0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

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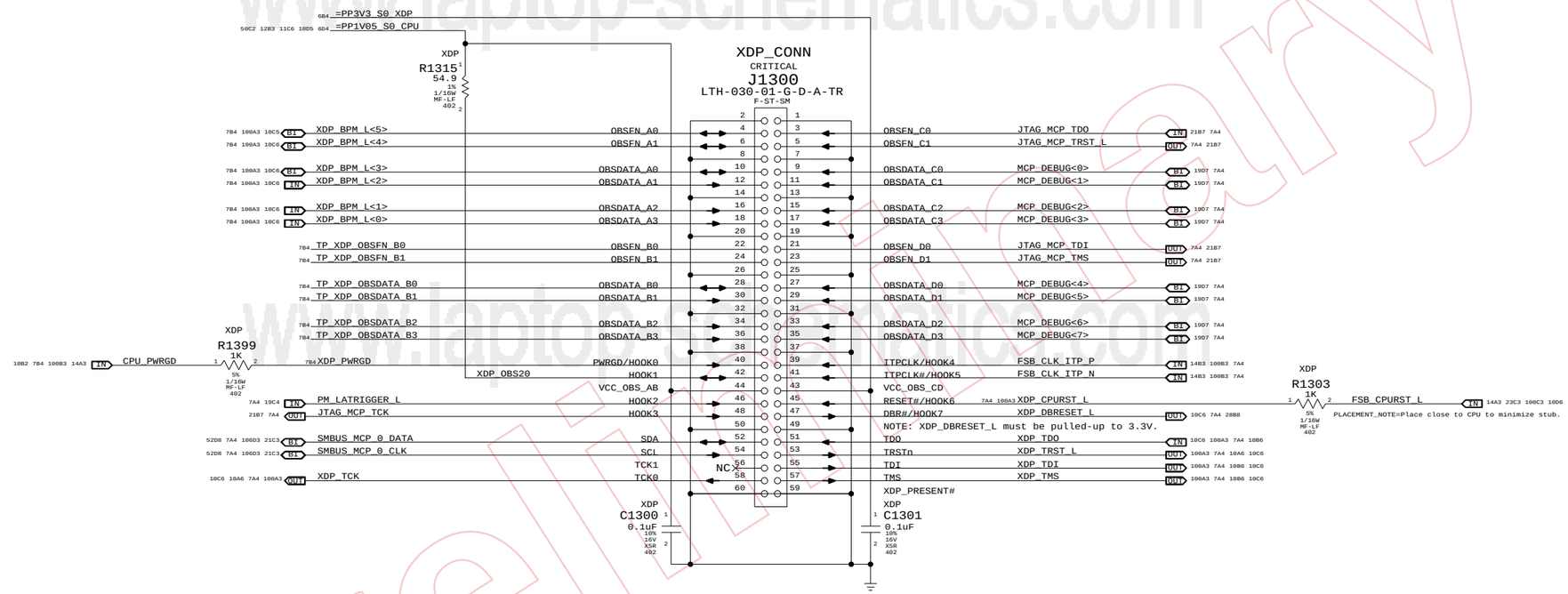
MCP79-specific pinout



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eXtended Debug Port (XDP)

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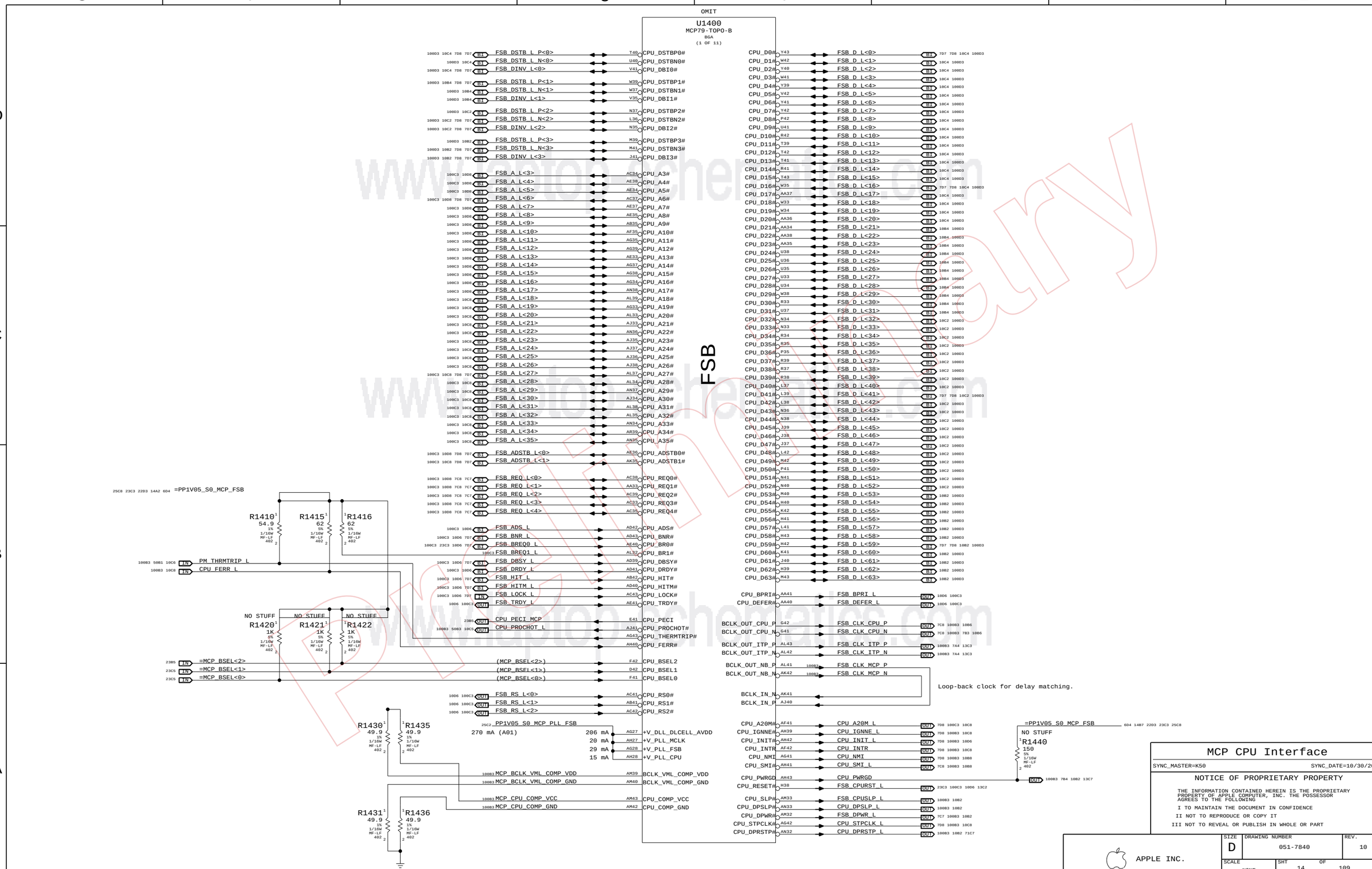

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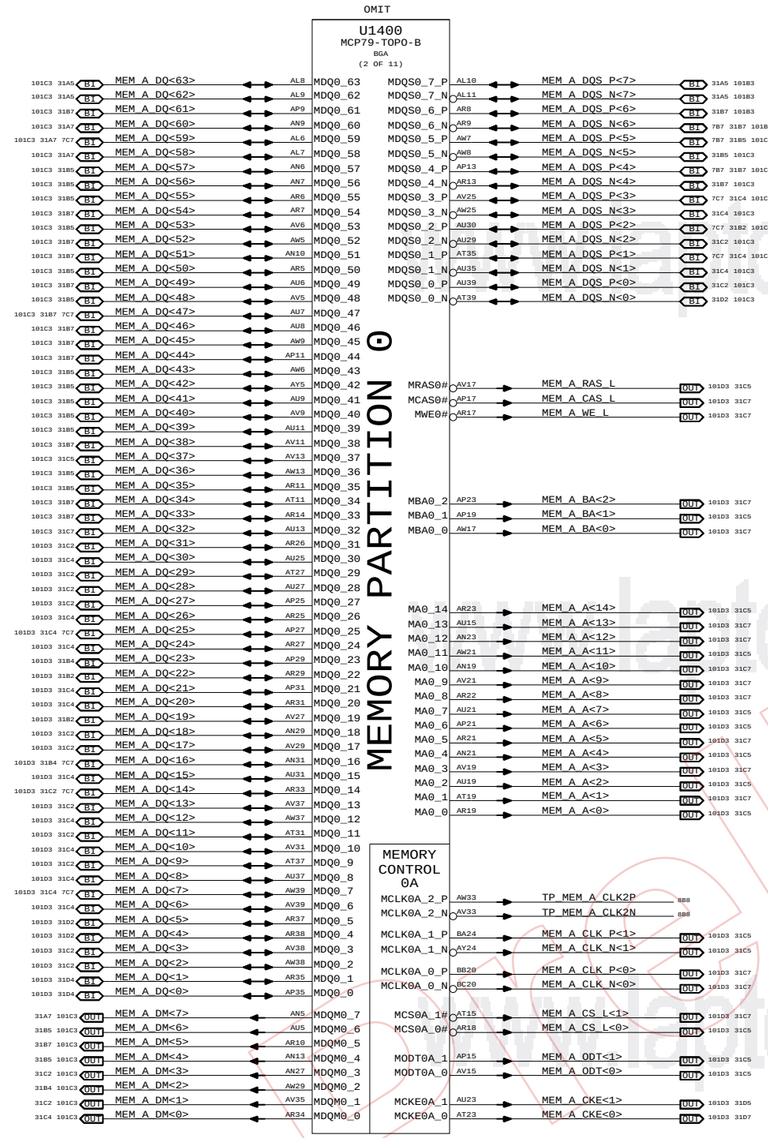

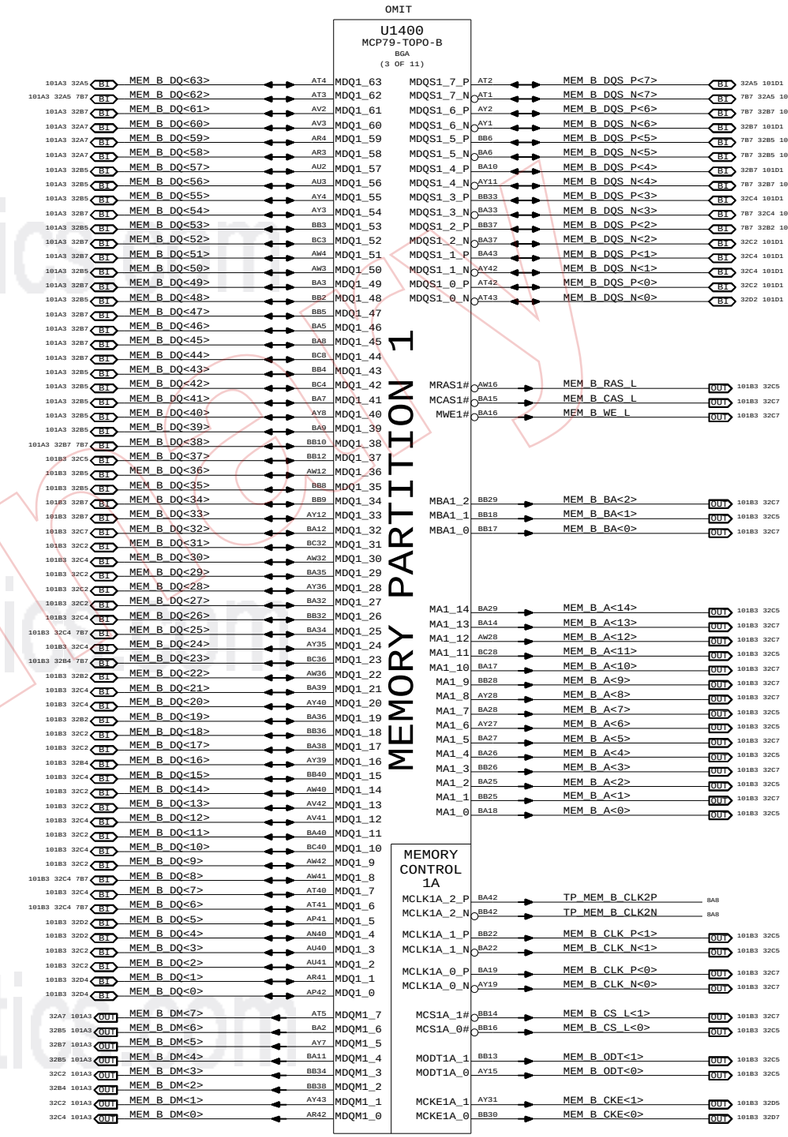

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MCP Memory Interface

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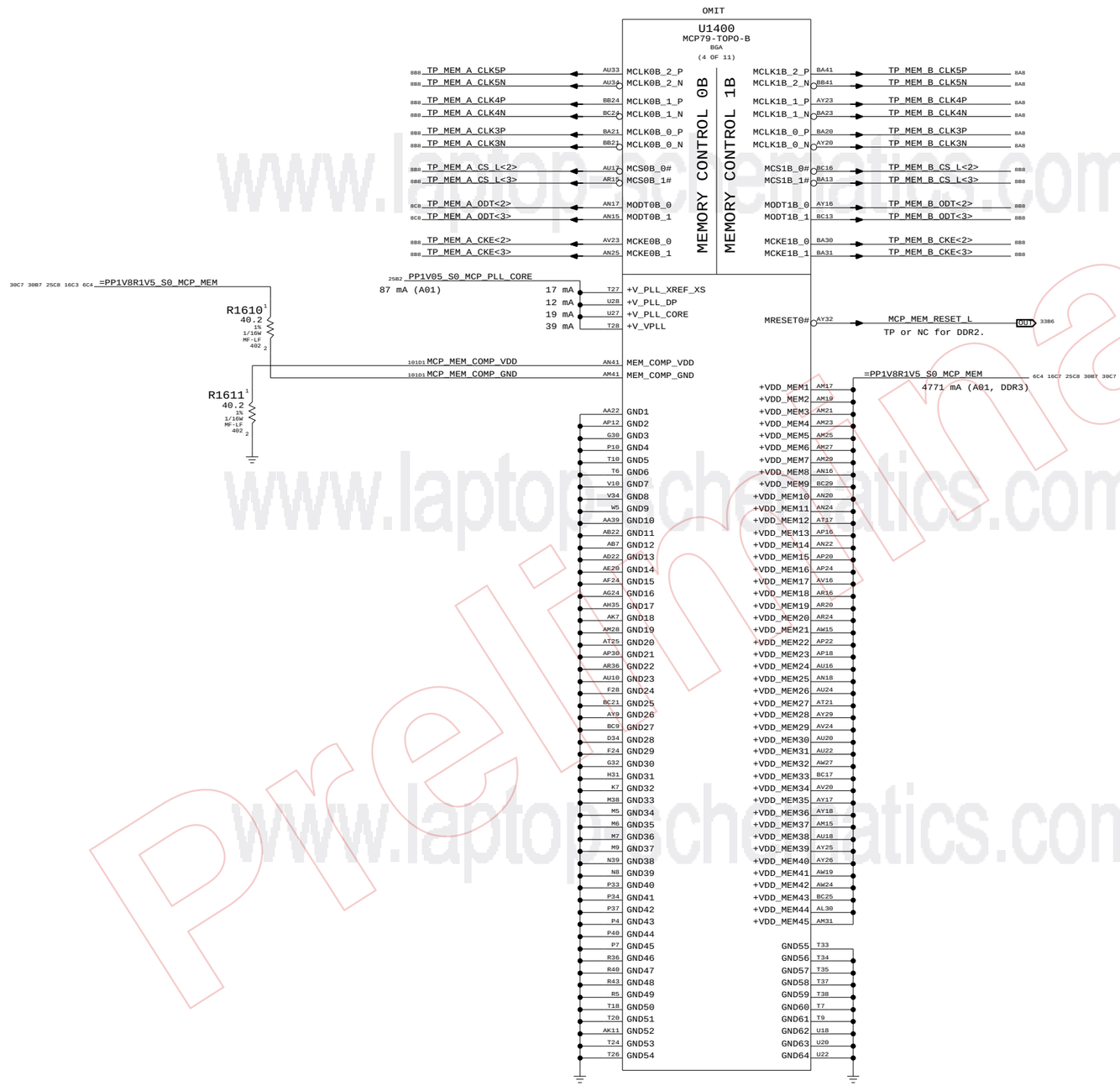

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MCP Memory Misc

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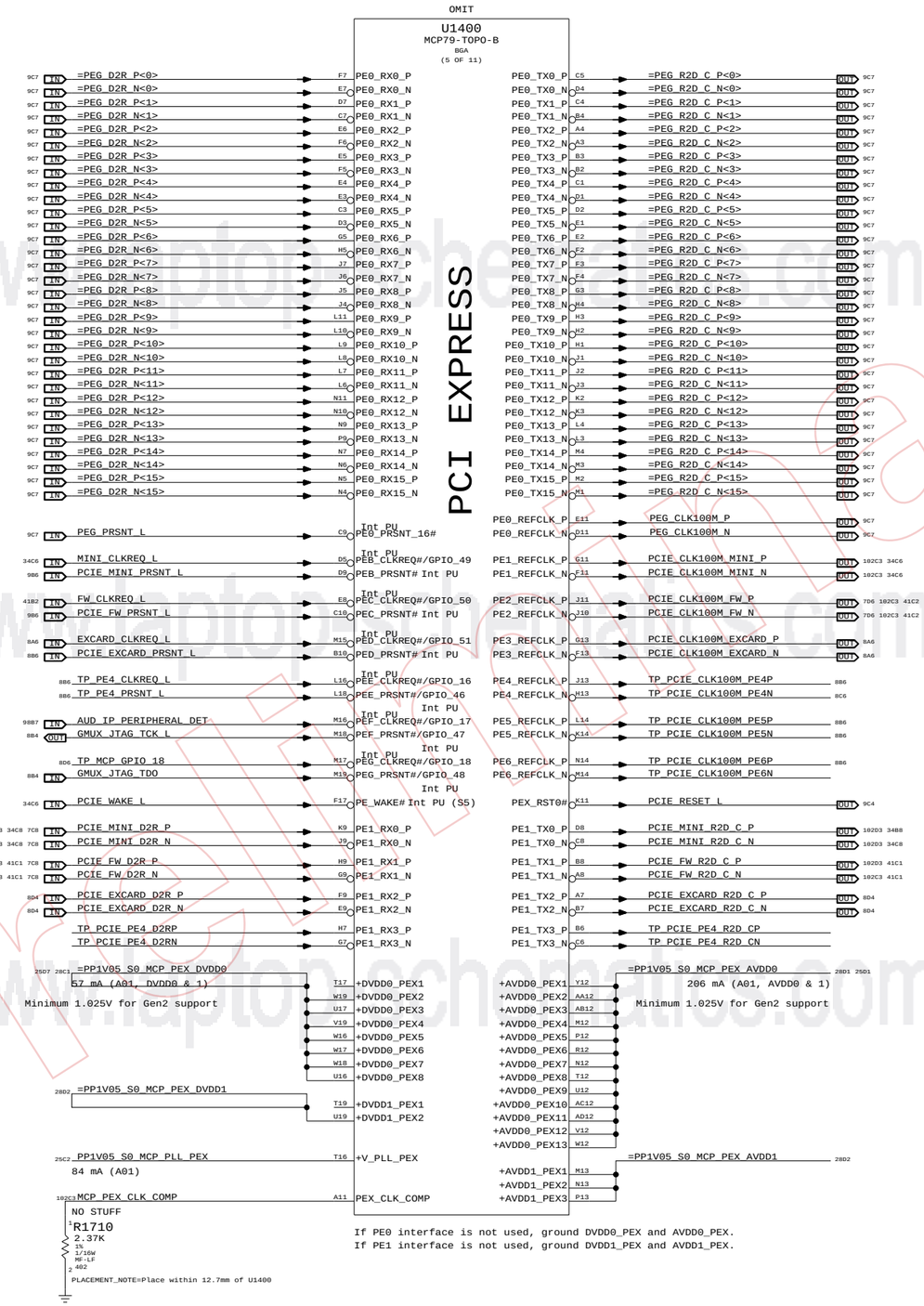

MCP PCIe Interfaces

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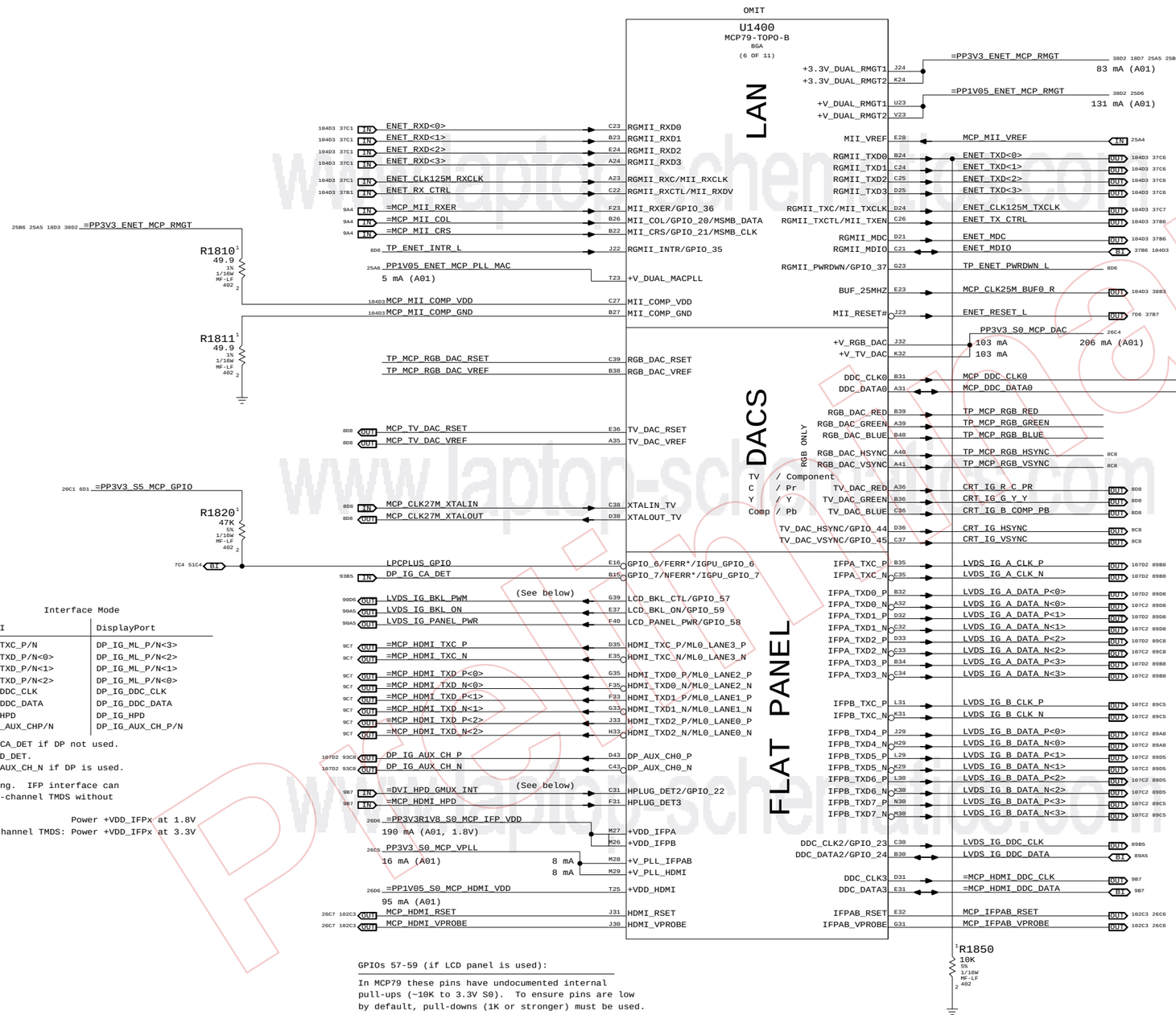

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

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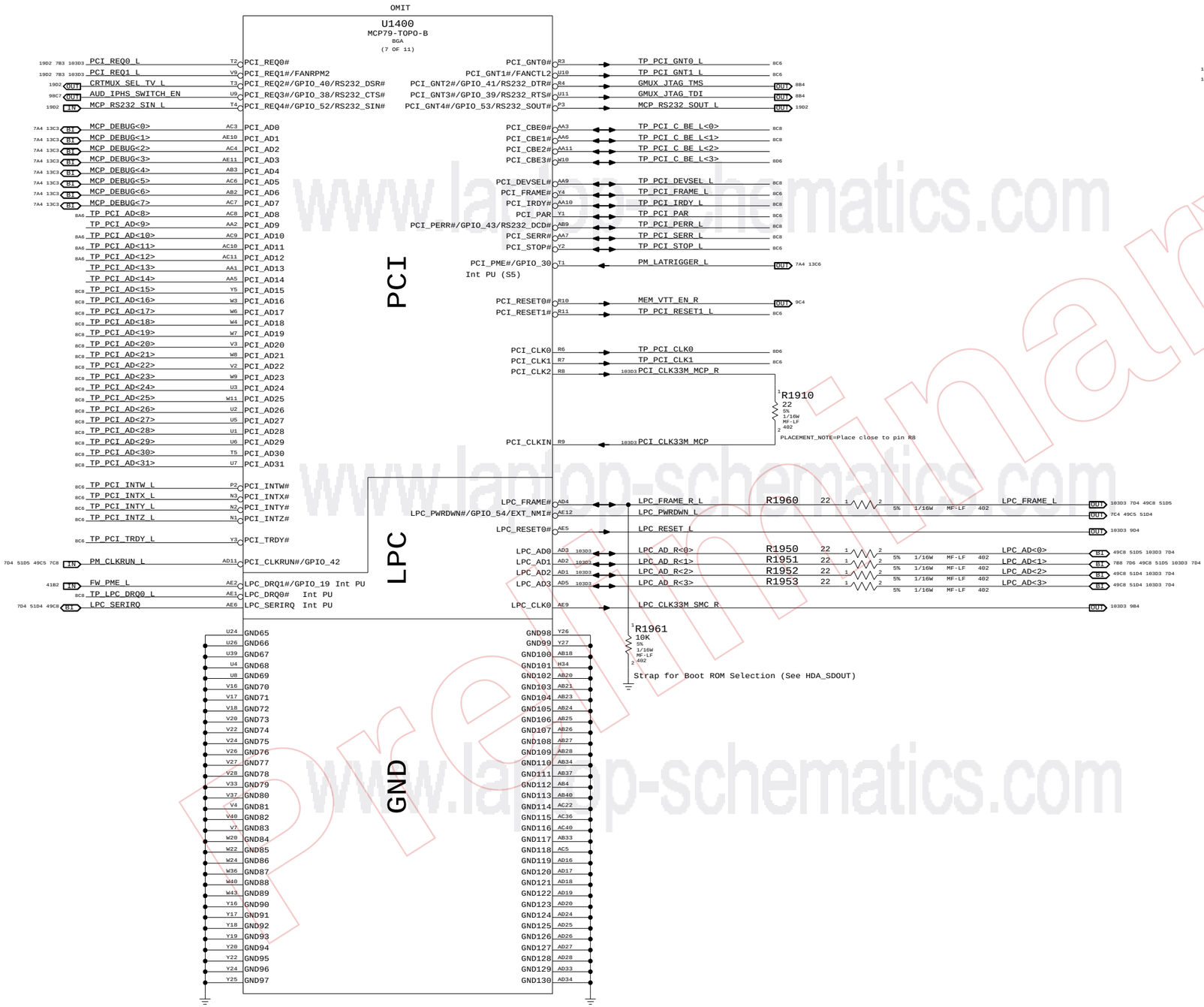

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MCP PCI & LPC

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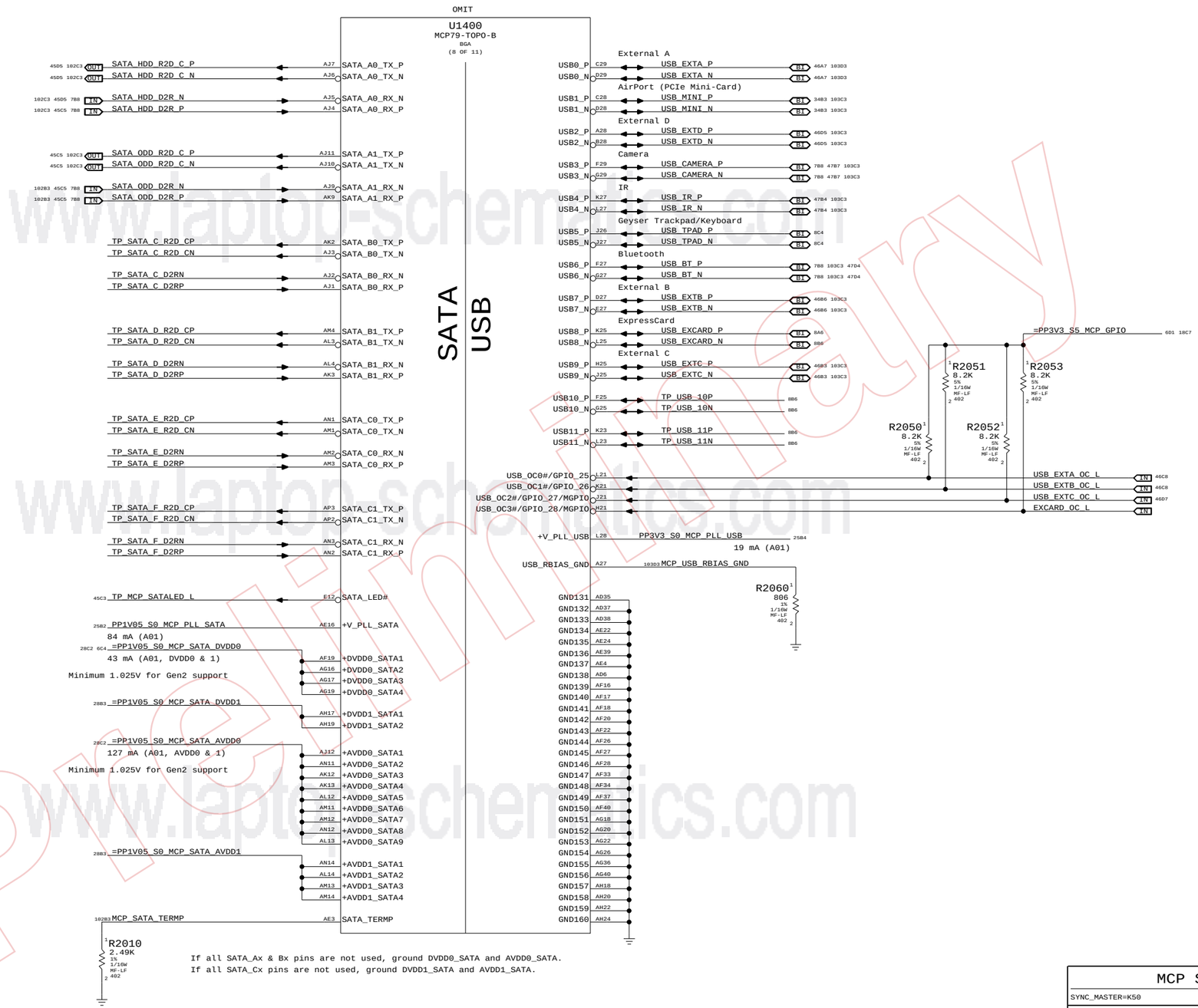

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB

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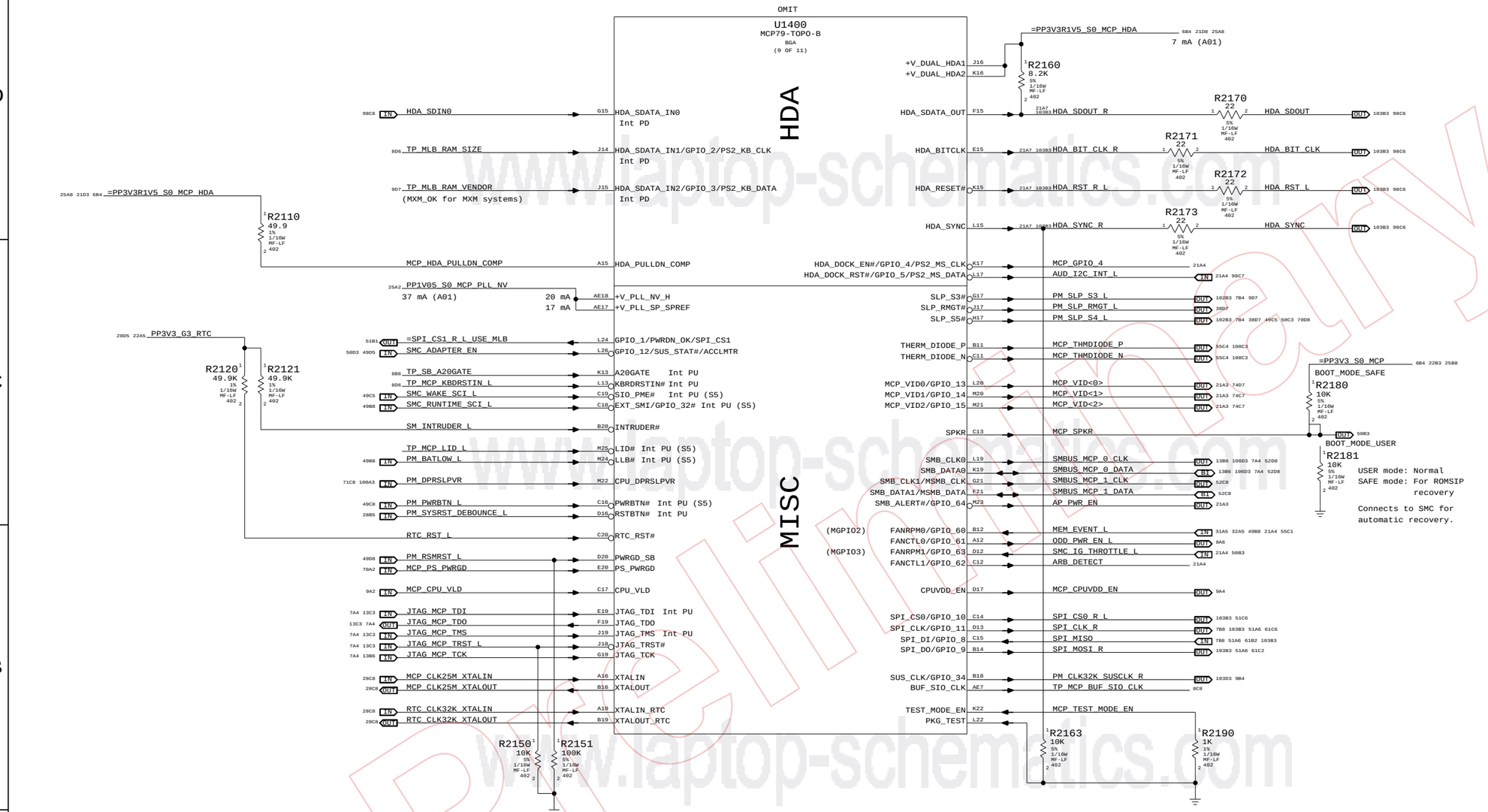


BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

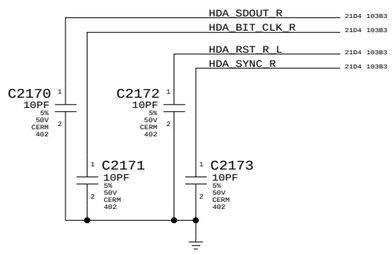
SPI Frequency Select

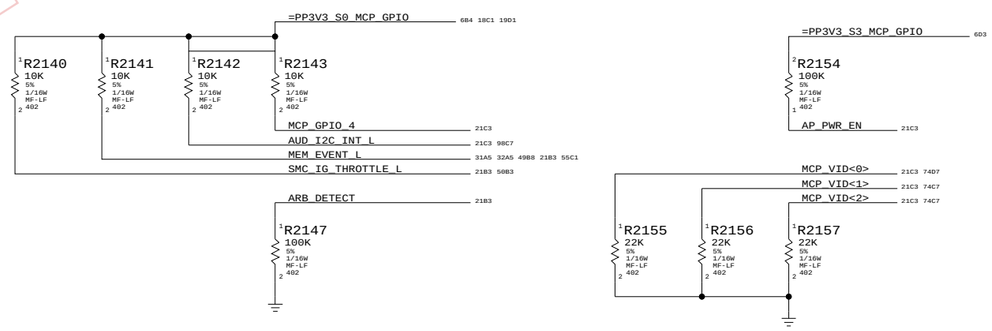
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface





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MCP HDA & MISC

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U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

25D8 6D4 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

=PP1V05_S0_MCP_FSB 6D4 14A2 14B7 23C3 25C8
1139 mA 1182 mA (A01)

AA25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	E40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AE32
AC16	+VDD_CORE13	+VTT_CPU13	AH32
AC17	+VDD_CORE14	+VTT_CPU14	AJ32
AC18	+VDD_CORE15	+VTT_CPU15	AK31
AC19	+VDD_CORE16	+VTT_CPU16	AK32
AC20	+VDD_CORE17	+VTT_CPU17	AD32
AC21	+VDD_CORE18	+VTT_CPU18	AL31
AA17	+VDD_CORE19	+VTT_CPU19	AB32
AC24	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AE19	+VDD_CORE30	+VTT_CPU30	F37
AE21	+VDD_CORE31	+VTT_CPU31	F38
AE23	+VDD_CORE32	+VTT_CPU32	F39
AE25	+VDD_CORE33	+VTT_CPU33	G36
AE26	+VDD_CORE34	+VTT_CPU34	G37
AE27	+VDD_CORE35	+VTT_CPU35	G38
AE28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CORE40	+VTT_CPU40	K33
AF21	+VDD_CORE41	+VTT_CPU41	K34
AF23	+VDD_CORE42	+VTT_CPU42	K35
AF25	+VDD_CORE43	+VTT_CPU43	L32
AF3	+VDD_CORE44	+VTT_CPU44	L33
AF4	+VDD_CORE45	+VTT_CPU45	L34
AF7	+VDD_CORE46	+VTT_CPU46	M31
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	N31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58		
AG7	+VDD_CORE59		
AG8	+VDD_CORE60		
AG9	+VDD_CORE61		
AH1	+VDD_CORE62		
AH10	+VDD_CORE63		
AH11	+VDD_CORE64		
W26	+VDD_CORE65		
AH2	+VDD_CORE66		
AA23	+VDD_CORE67		
W28	+VDD_CORE68		
AH25	+VDD_CORE69		
AH21	+VDD_CORE70	+3.3V_DUAL1	G18
AH3	+VDD_CORE71	+3.3V_DUAL2	H19
AH4	+VDD_CORE72	+3.3V_DUAL3	J20
AH5	+VDD_CORE73	+3.3V_DUAL4	K20
AH6	+VDD_CORE74		
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
		+VDD_AUXC1	T21
		+VDD_AUXC2	U21
A20	+VBAT	+VDD_AUXC3	V21

43 mA

=PP3V3_S0_MCP 6B4 21C2 25B8
450 mA (A01)

=PP3V3_S5_MCP 6D1 25B8
16 mA 266 mA (A01)

250 mA

=PP1V05_S5_MCP_VDD_AUXC 6D1 25D8
105 mA (A01)

28D5 21C8 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

Preliminary
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MCP Power & Ground

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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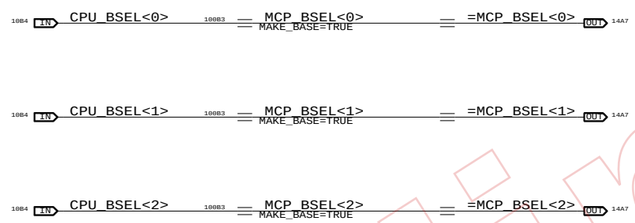
D	051-7840	10

SCALE NONE SHT 22 OF 109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

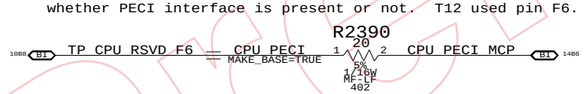
CPU FSB Frequency Straps



BSEL<2..0>	FSB MHz
000	266
001	133
010	200
011	(166)
100	333
101	100
110	(400)
111	(RSVD)

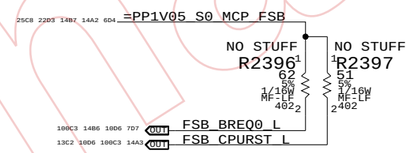
NOTE: () values not supported by MCP79.

Merom/Penryn do not officially support PECI, but it's not clear whether PECI interface is present or not. T12 used pin F6.



Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa



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Debug: CPU

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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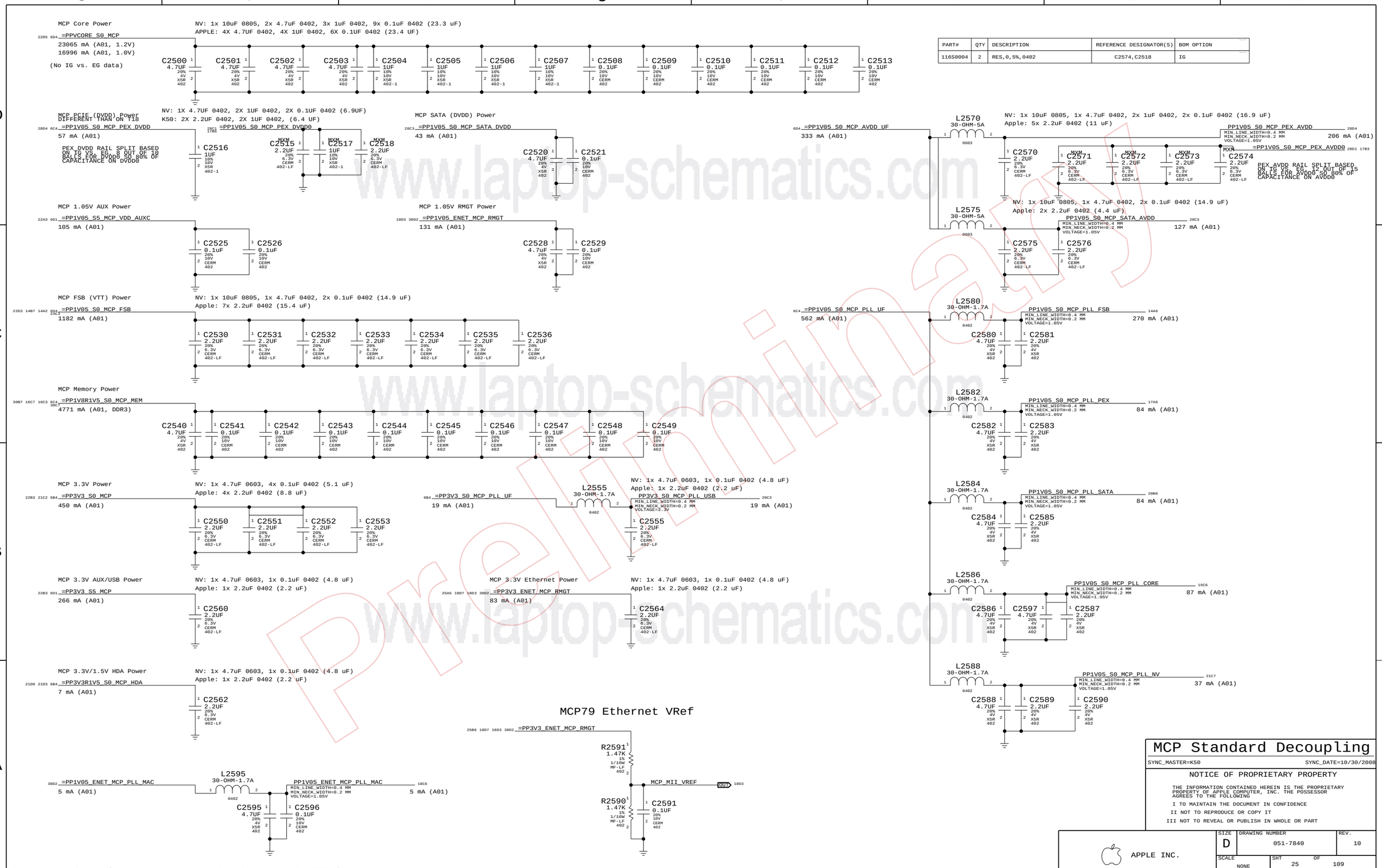

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

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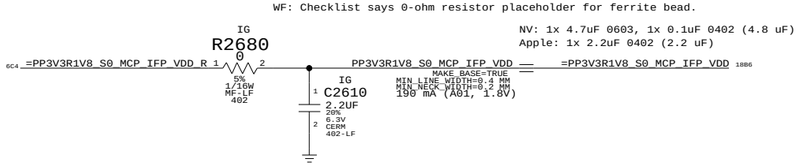
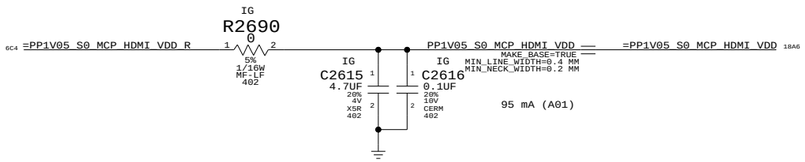
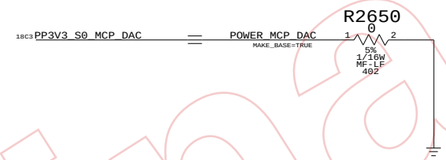
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



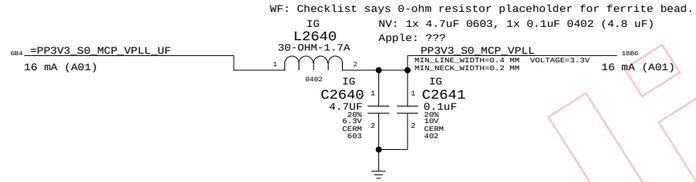
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM



WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

Preliminary

MCP Graphics Support

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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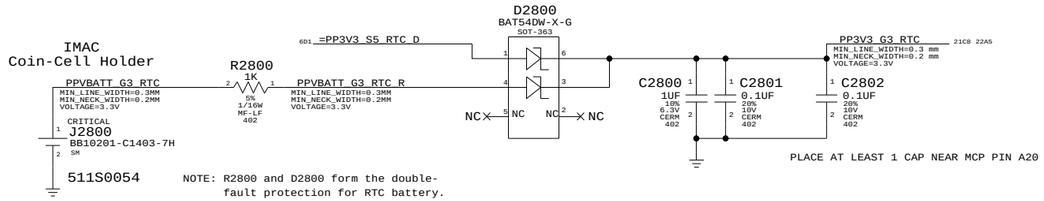
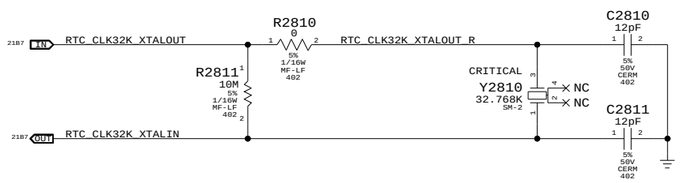
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

RTC Power Sources

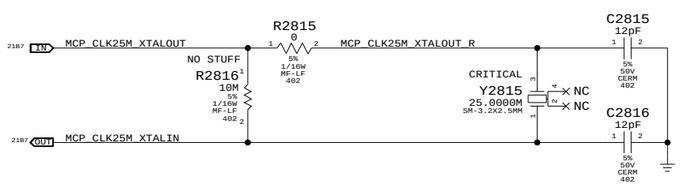


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

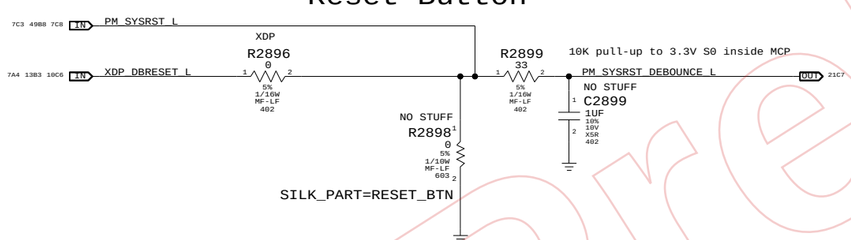
RTC Crystal



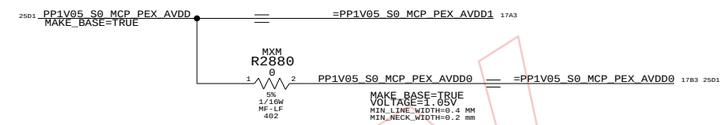
MCP 25MHz Crystal



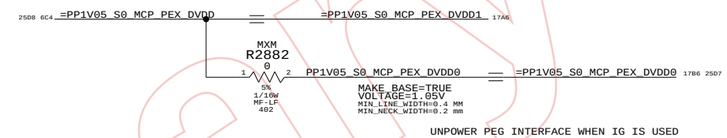
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN



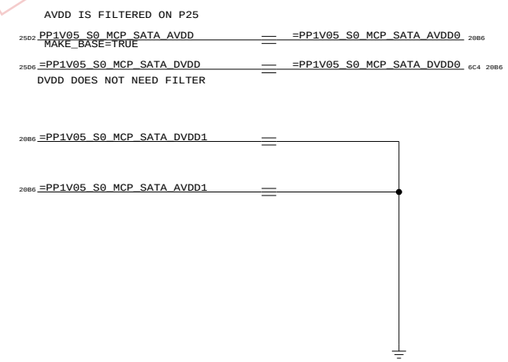
UNPOWER PEG INTERFACE WHEN IG IS USED



UNPOWER PEG INTERFACE WHEN IG IS USED

SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1

AVDD IS FILTERED ON P25



Preliminary

SB Misc

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE NONE SHT 28 OF 109

Page Notes

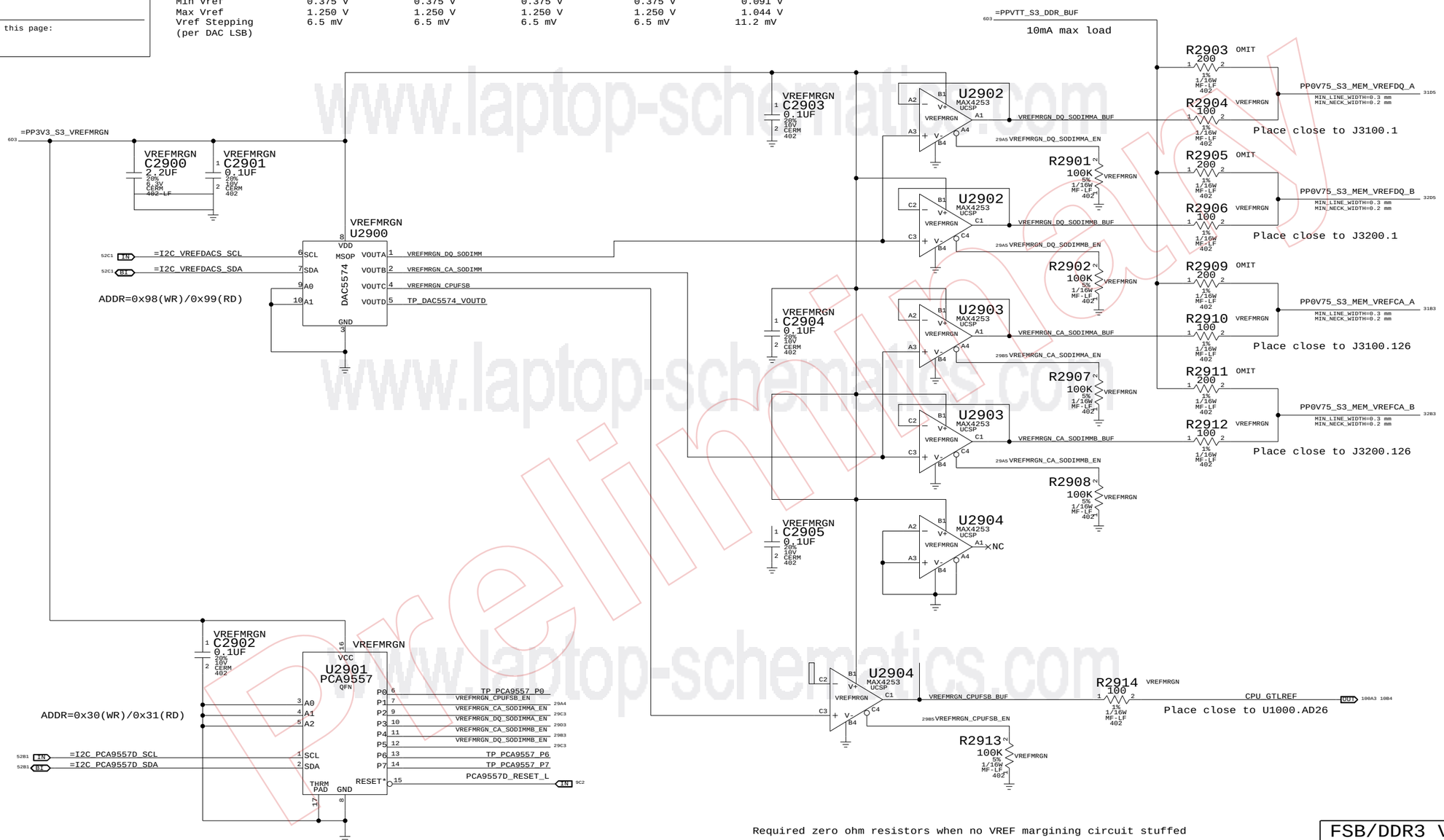
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2903		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2903		PRODUCTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2905		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2905		PRODUCTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2909		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2909		PRODUCTION
114S0149	1	RES,402,1/16W,200 OHM,1%	R2911		VREFMRGN
116S0004	1	RES,402,1/16W,0 OHM,5%	R2911		PRODUCTION

FSB/DDR3 Vref Margining

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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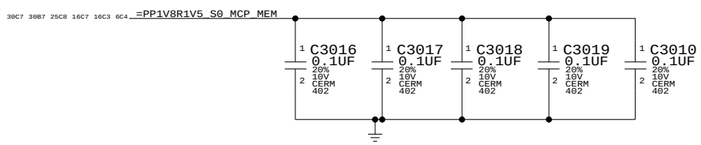
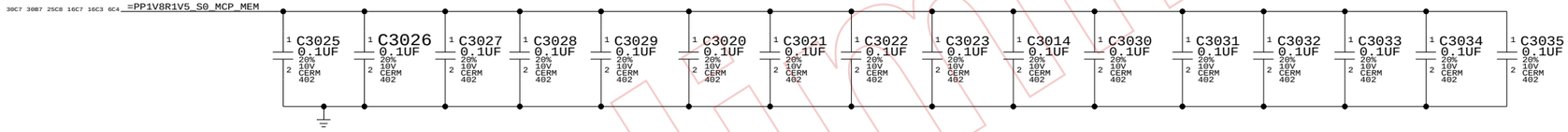
CAPS TO COUPLE MCP 1V5_S0_MEM AND DIMMS 1V5_S3

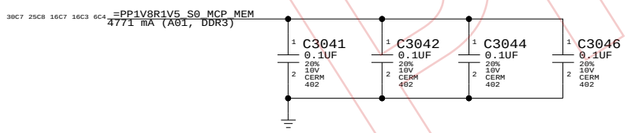
CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM A (FURTHER FROM MCP)



CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM B (CLOSER TO MCP)



EXTRA DECOUPLING CAPS FOR MCP MEM RAIL



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MEMORY COUPLING CAPS

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D	051-7840	10

SCALE NONE SHT 30 OF 109

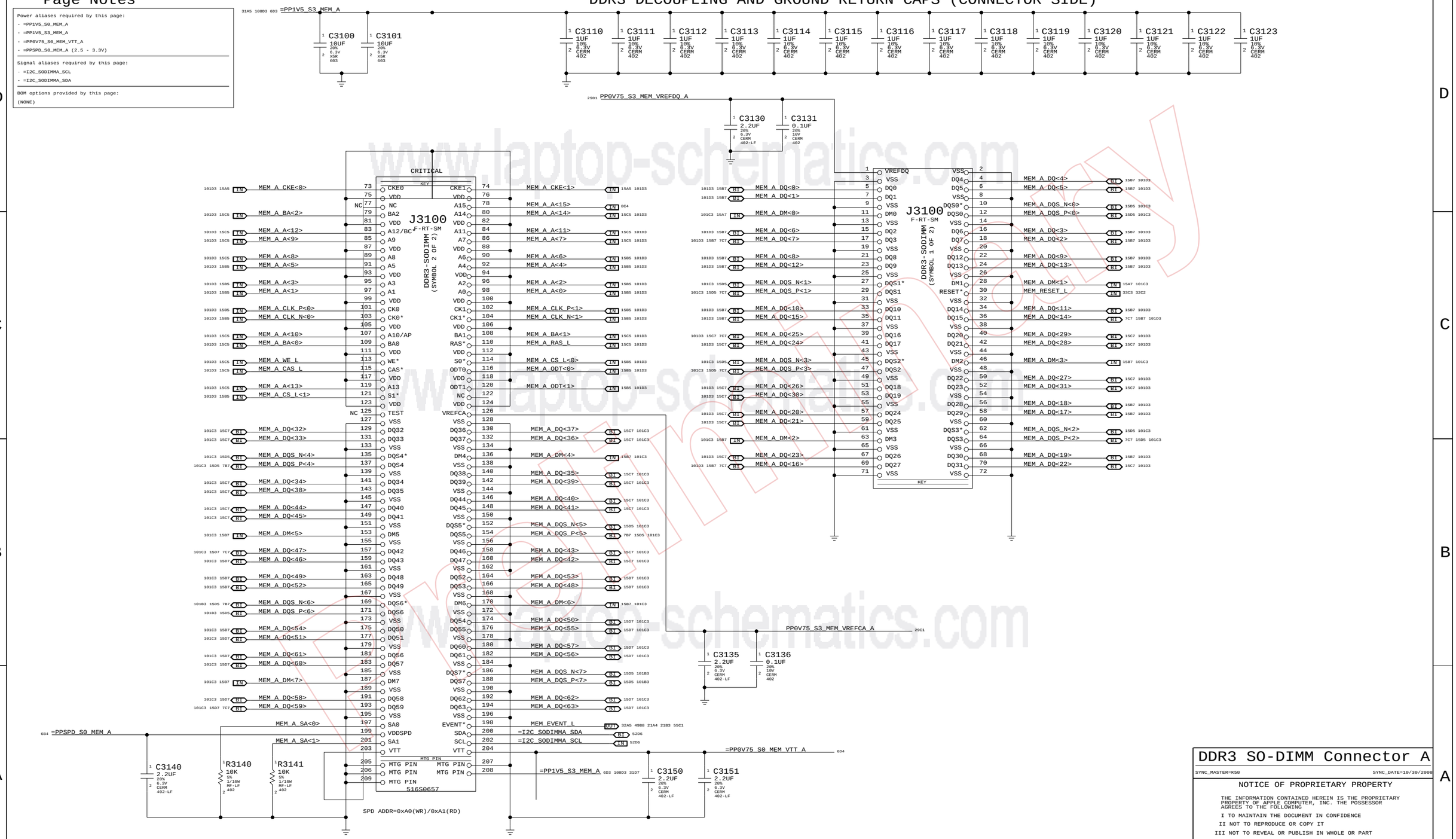
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 SO-DIMM Connector A

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

SCALE NONE — SHT 31 OF 109

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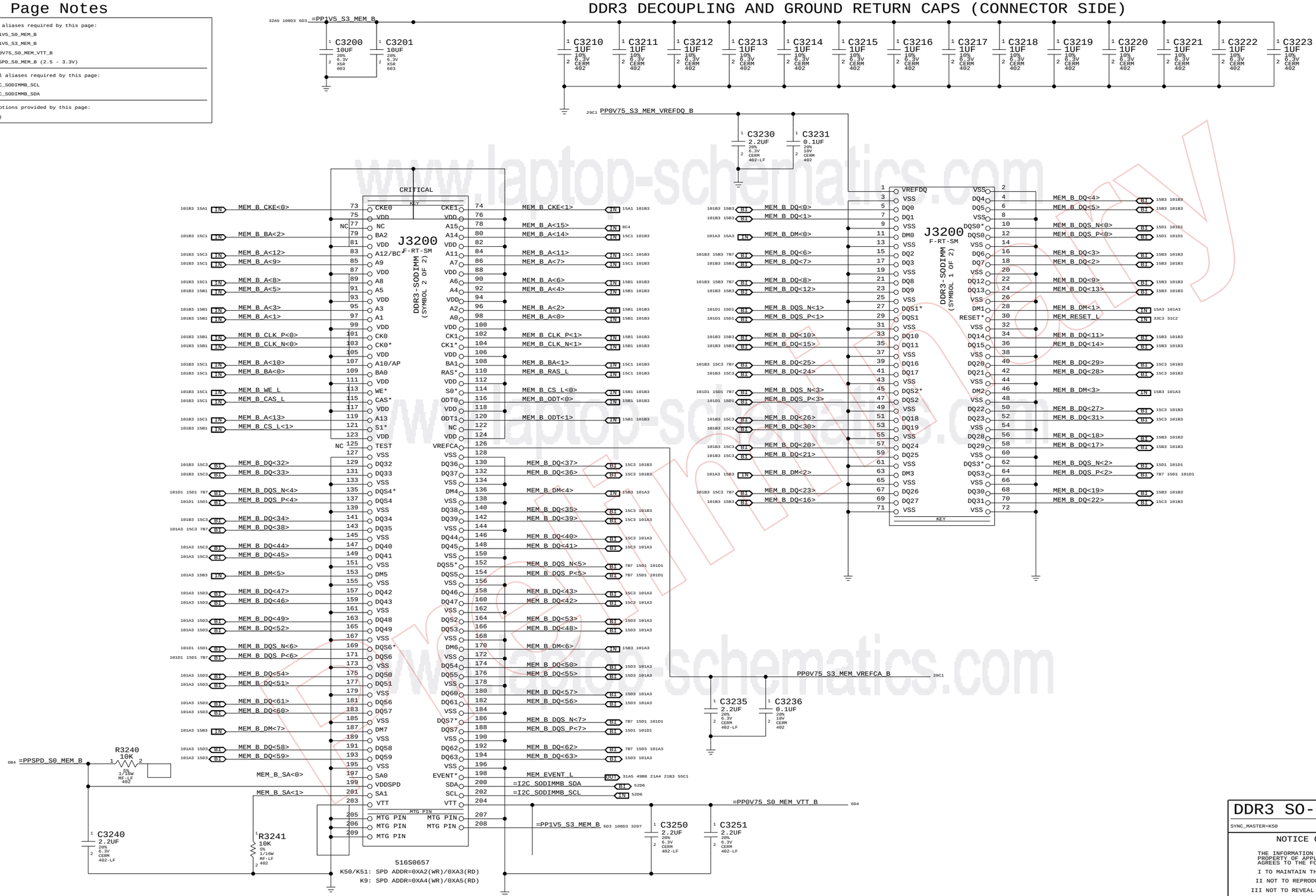
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 SO-DIMM CONNECTOR B

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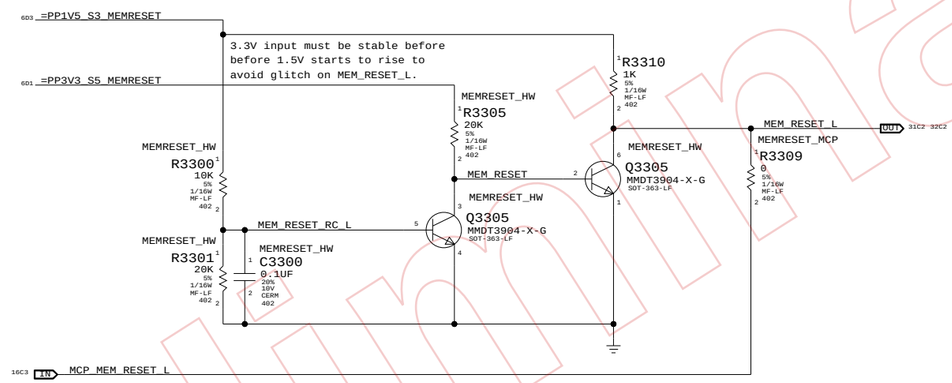
DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



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DDR3 Support

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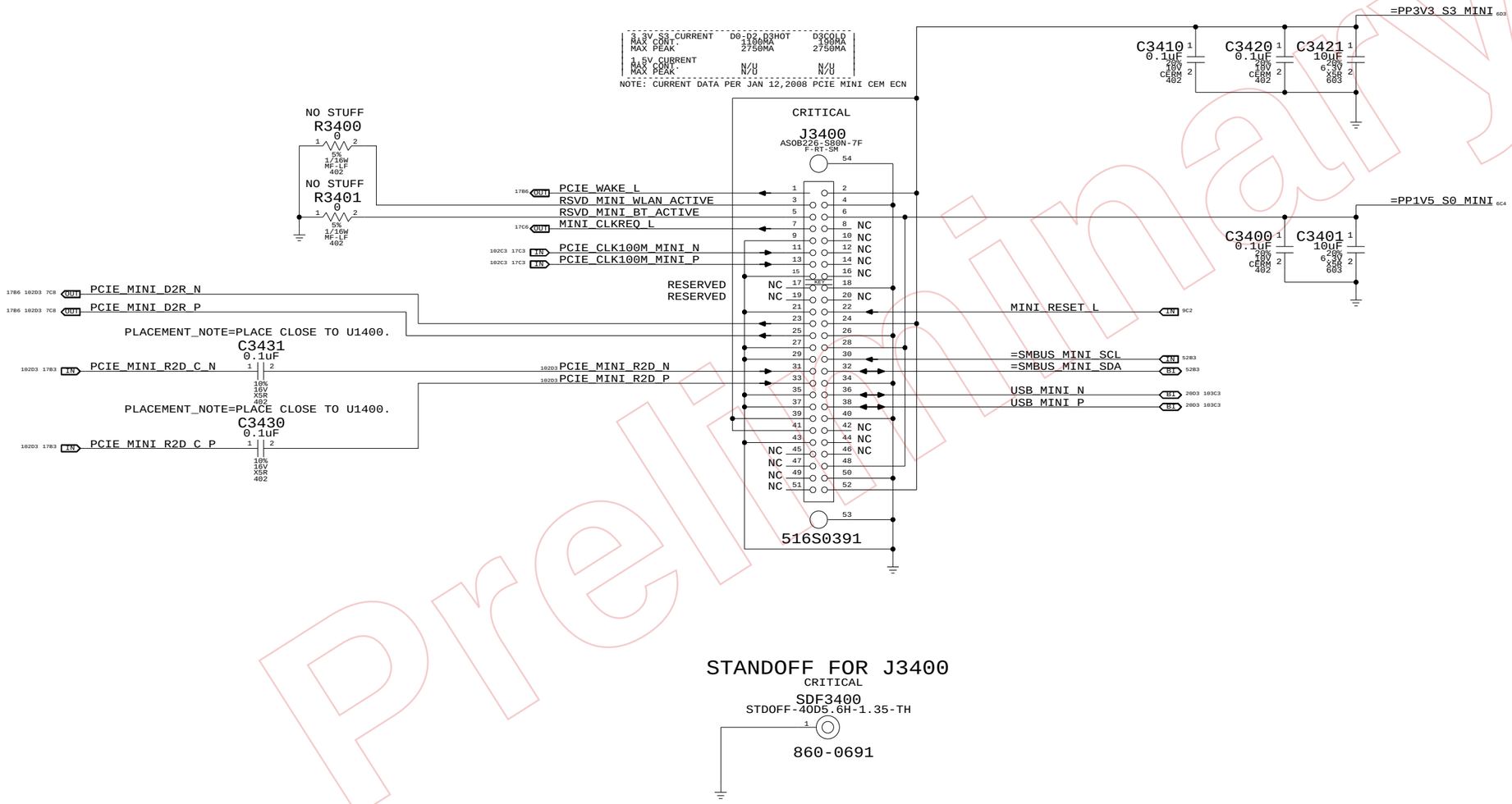
D	051-7840	10
SCALE NONE	SHT 33 OF 109	



STANDOFF FOR J3400

CRITICAL

SDF3400

STDOFF-4OD5.6H-1.35-TH

860-0691

Preliminary

PCI-E MiniCard Connector

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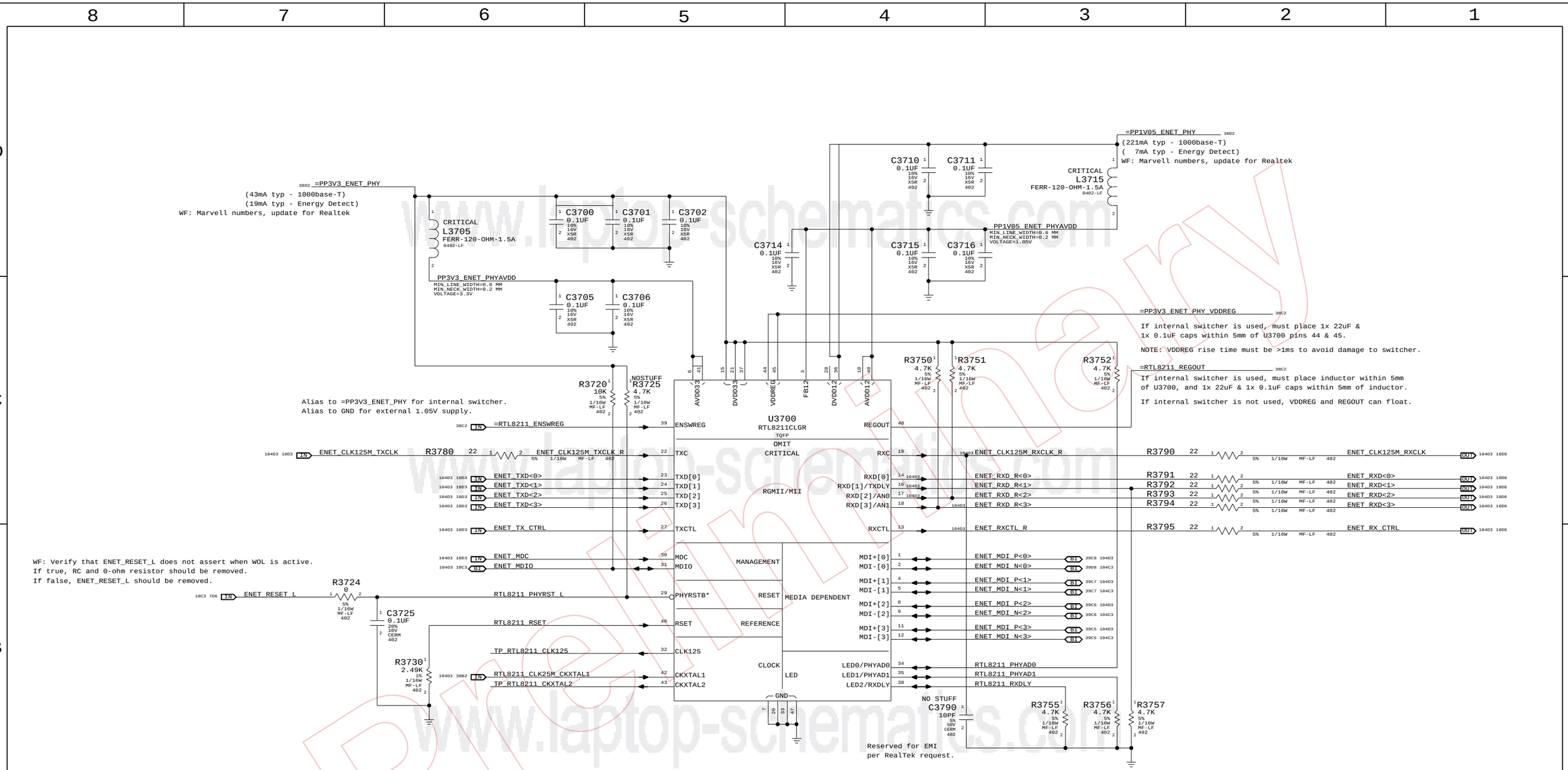
SCALE NONE	SHT 34 OF 109	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

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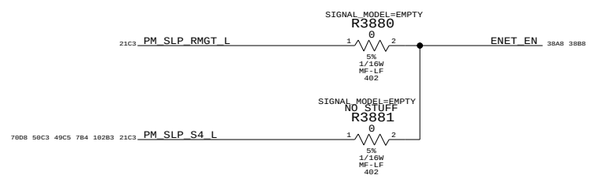
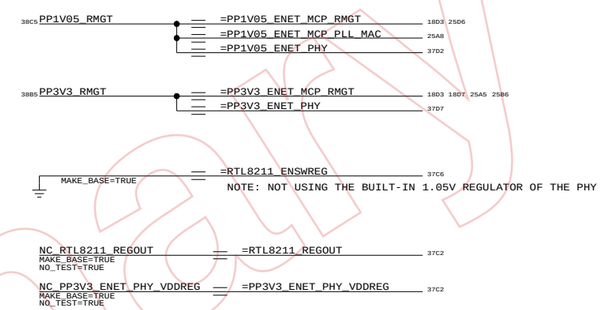
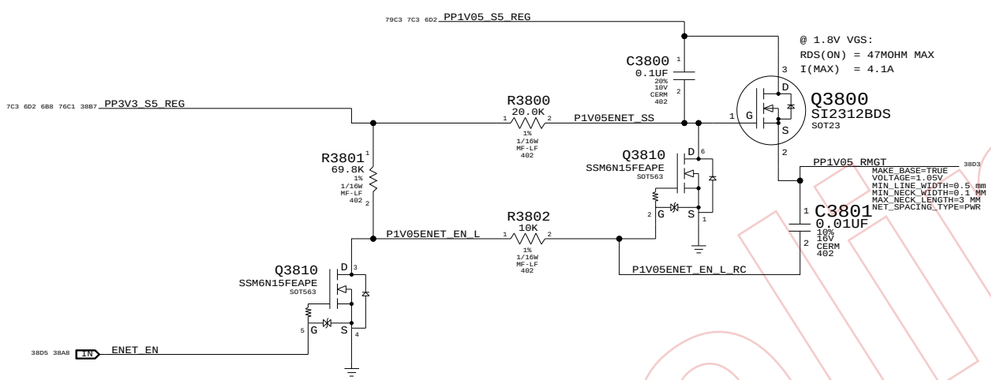
SOURCE SELECT



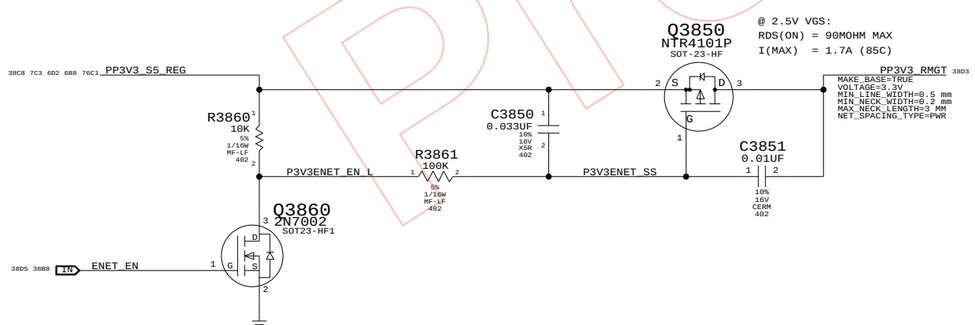
ENET ALIASES



1.05V ENET FET

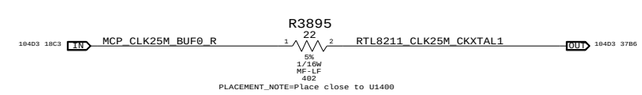


3.3V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



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Ethernet & AirPort Support

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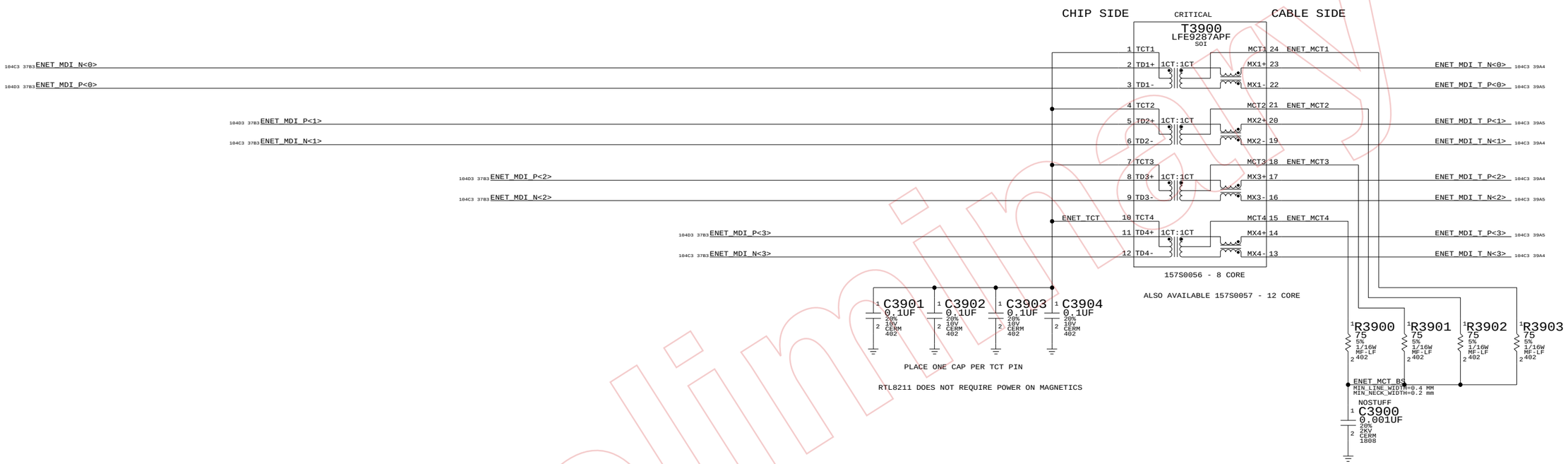
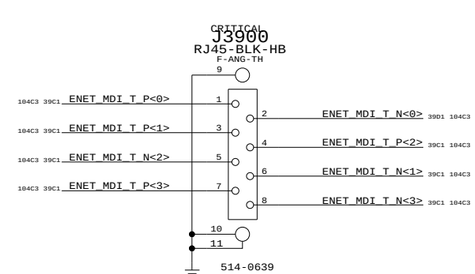
SCALE NONE	SHT 38 OF 109	

NOTE: DELTA RECOMMENDS CENTER-TAP BE FLOATING WHEN USING REALTEK PHY.



NOTE: BOB SMITH TERMINATION FOR EMC INVESTIGATION.



ETHERNET CONNECTOR

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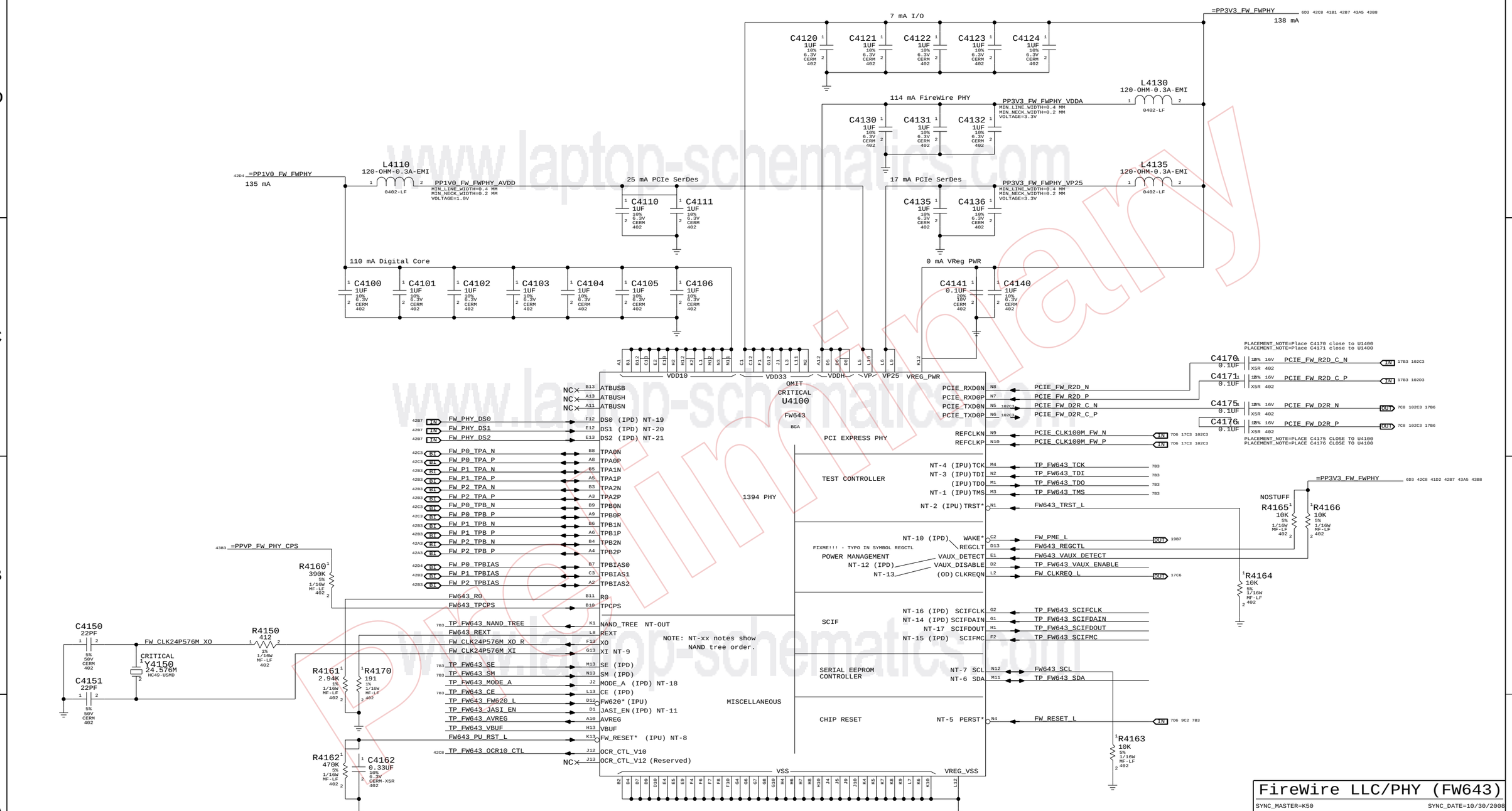

FireWire LLC/PHY (FW643)

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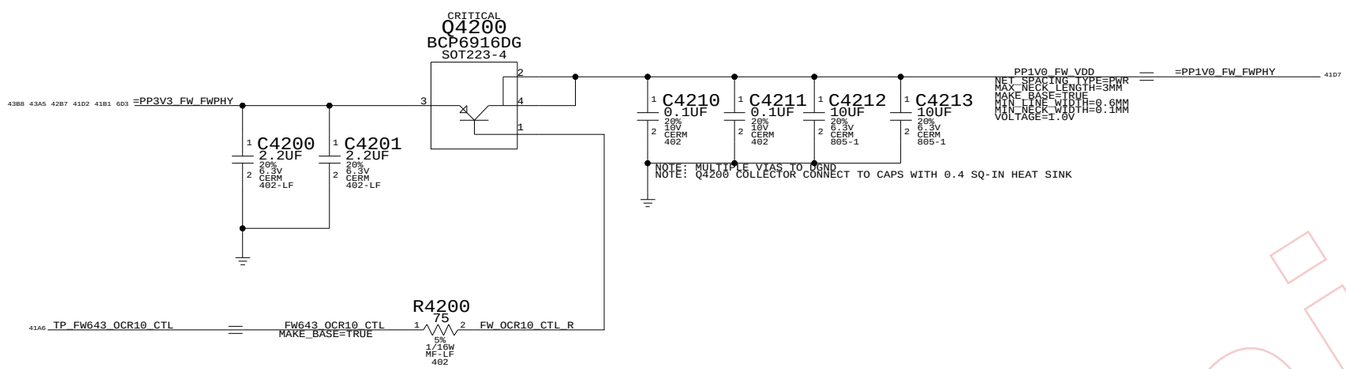
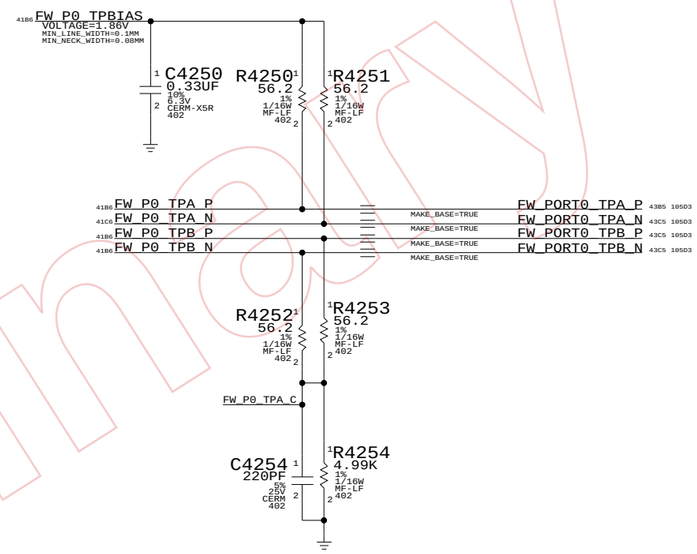
FW643 1.0V GENERATION

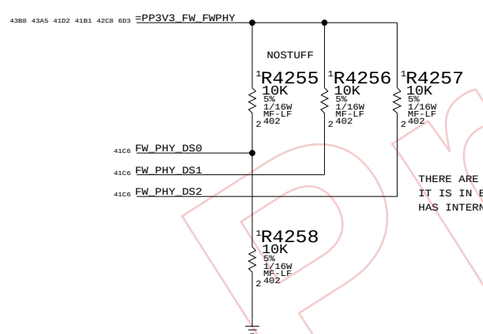


Termination

Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

41B6 FW_P1_TPBIAS — NC_FW_PORT1_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P1_TPA_P — NC_FW_PORT1_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P1_TPA_N — NC_FW_PORT1_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P1_TPB_P — NC_FW_PORT1_TPB_P (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P1_TPB_N — NC_FW_PORT1_TPB_N (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P2_TPBIAS — NC_FW_PORT2_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P2_TPA_P — NC_FW_PORT2_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P2_TPA_N — NC_FW_PORT2_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P2_TPB_P — NC_FW_PORT2_TPB_P (MAKE_BASE=TRUE, NO_TEST=TRUE)
41B6 FW_P2_TPB_N — NC_FW_PORT2_TPB_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

Preliminary

FW: 1394B MISC

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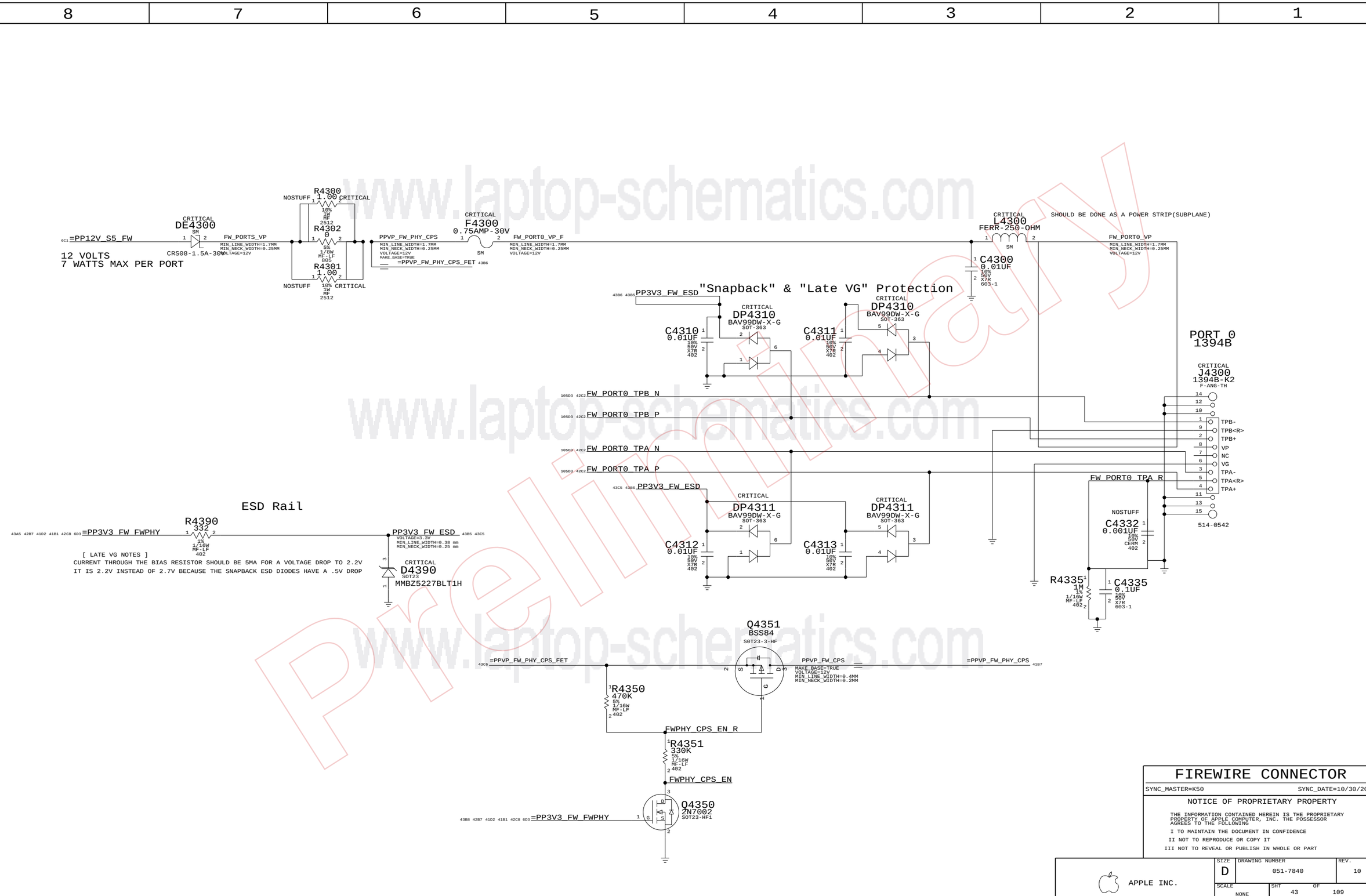

FIREWIRE CONNECTOR

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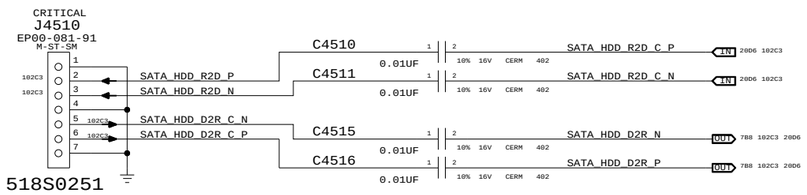
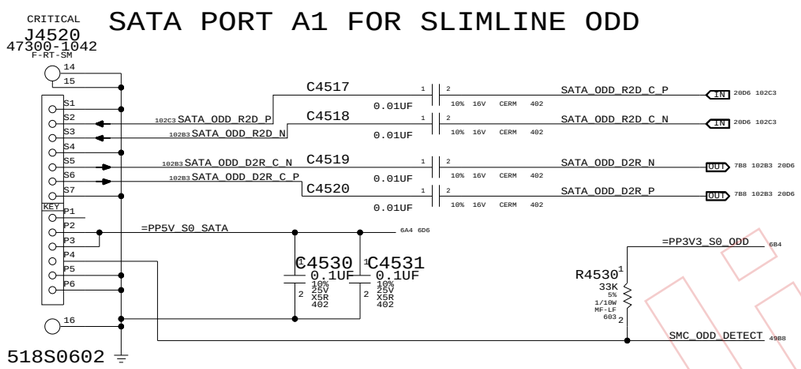
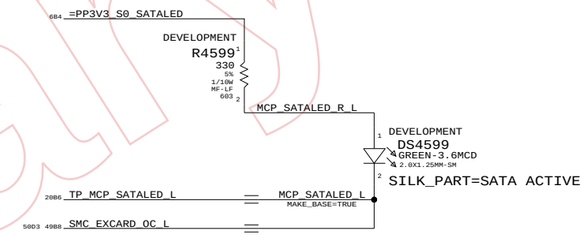
SATA PORT A0 FOR HDD



SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



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SATA Connectors

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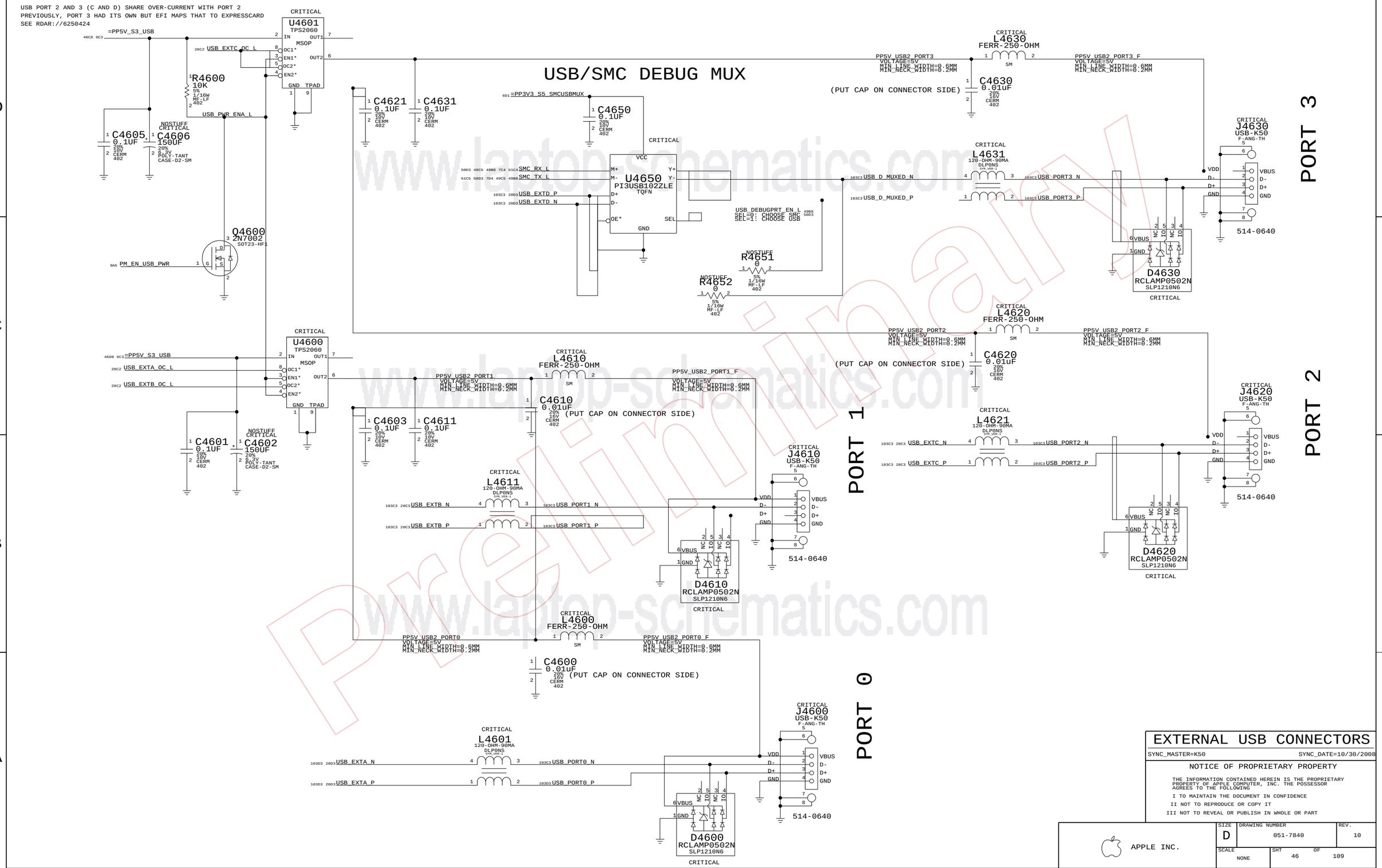
USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD ITS OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

USB/SMC DEBUG MUX



EXTERNAL USB CONNECTORS

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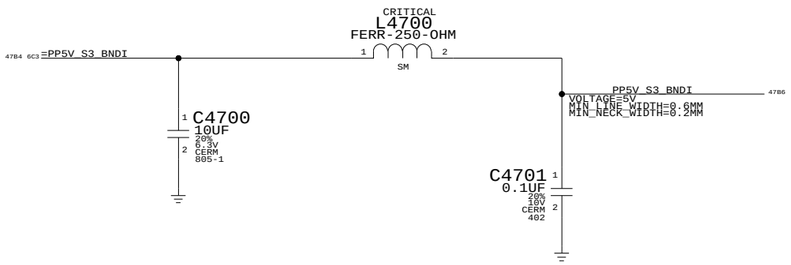
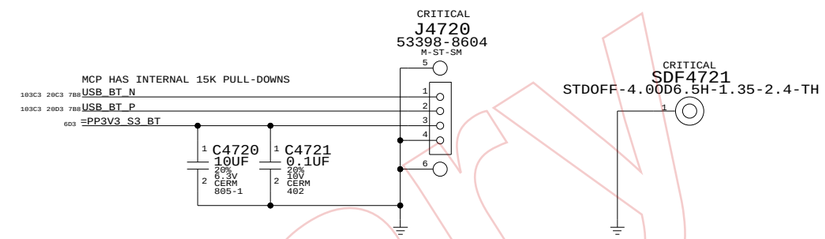
CAMERA POWER FILTERING

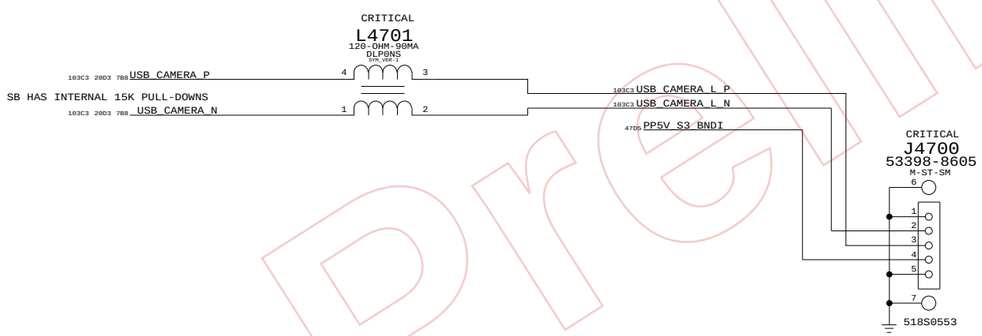


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

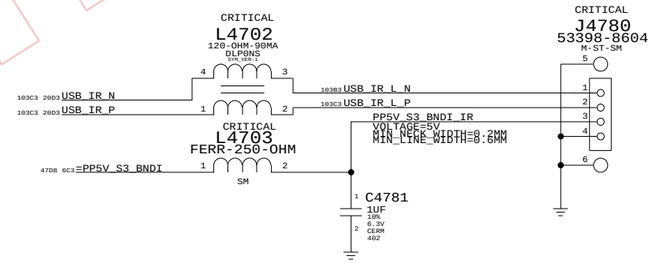
K37L (BLUETOOTH) CONNECTOR

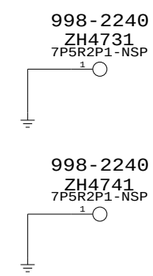


CAMERA CONNECTOR



IR RECEIVER





Preliminary

Internal USB Connections

SYNC_MASTER=K51 SYNC_DATE=07/09/2008

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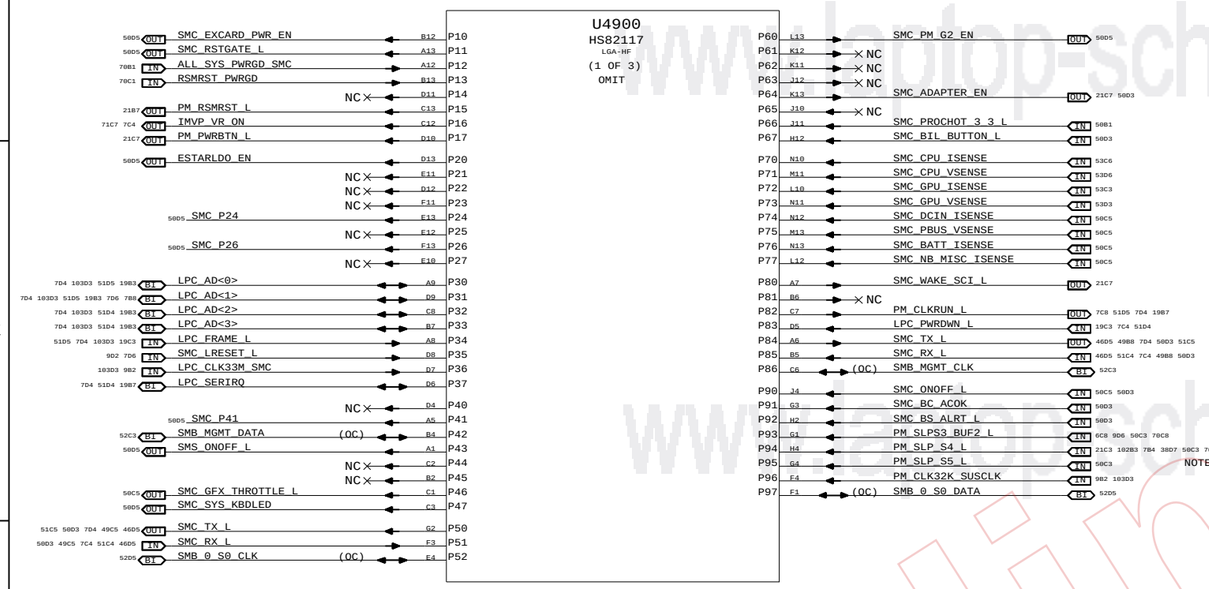
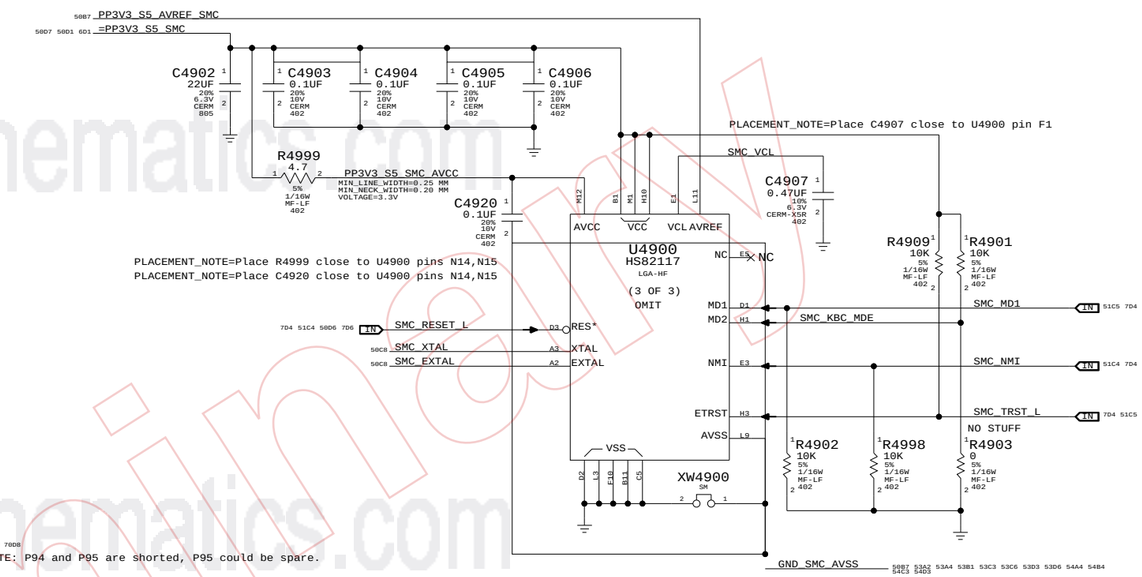
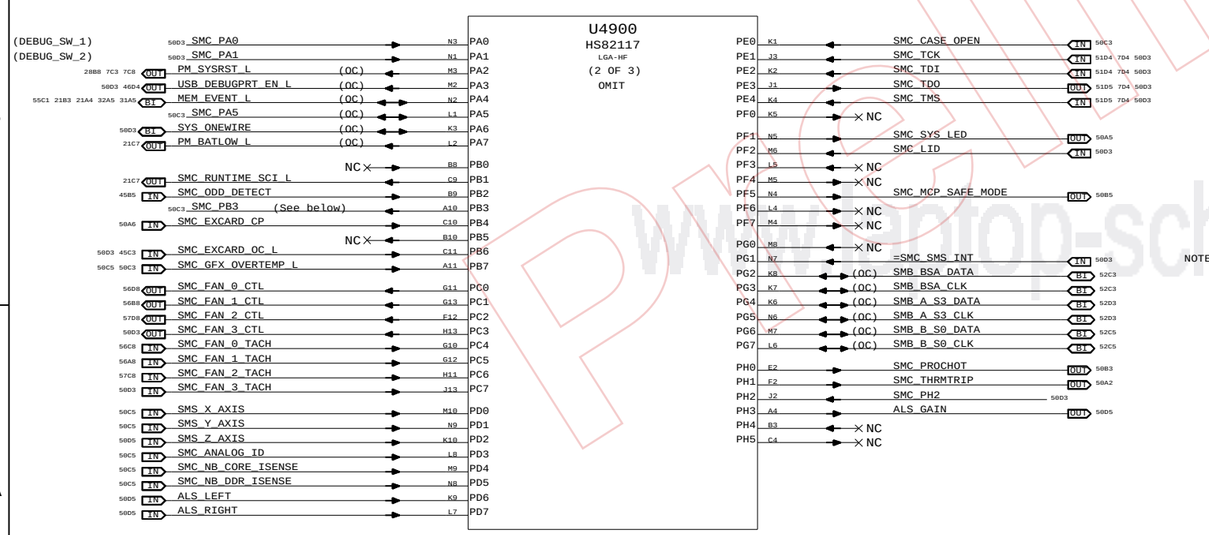
SCALE NONE	SHT 47 OF 109	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.





NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

BROKE SYNC FROM T18 ON 7/1/08; K50 NOW MASTER

SMC

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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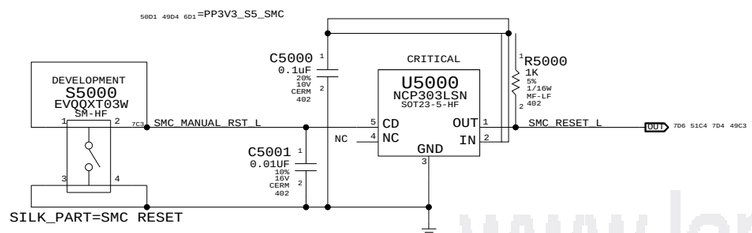
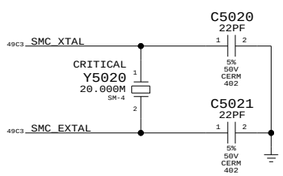
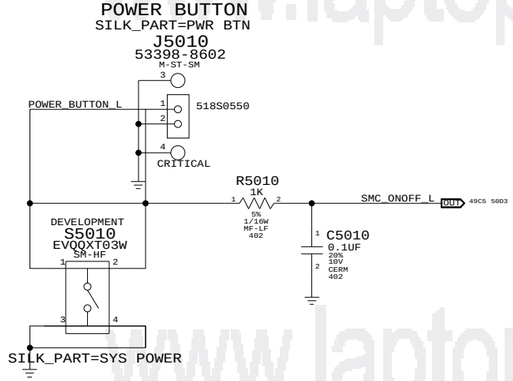
SMC Reset Button / Brownout Detect



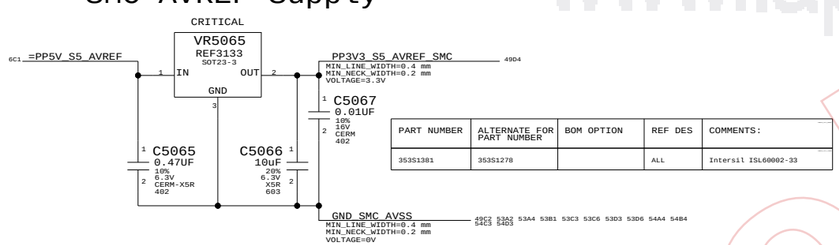
SMC Crystal Circuit



POWER BUTTON

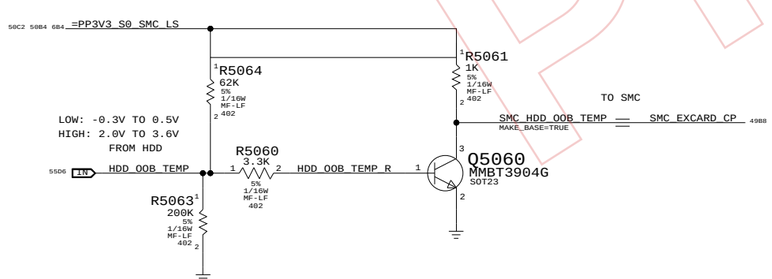


SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

SMS_Z_AXIS	NC_SMS_Z_AXIS	NO_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	
ALS_RIGHT	TP_ALS_RIGHT	

UNUSED TP/NC ALIASES

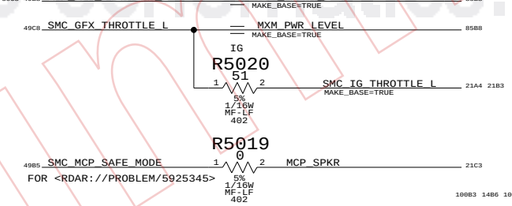
ALS_GAIN	NC_ALS_GAIN	NO_TEST=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	
SMS_ONOFF_L	TP_SMS_ONOFF_L	
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	
SMC_P24	TP_SMC_P24	
SMC_P26	TP_SMC_P26	
SMC_P41	TP_SMC_P41	
ESTARLDO_EN	TP_ESTARLDO_EN	

ANALOG SENSORS

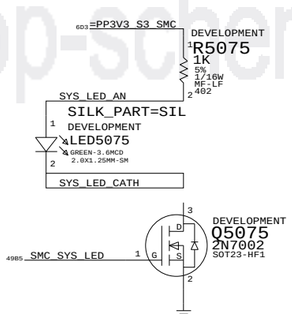
SMC_DCIN_ISENSE	SMC_12V_S0_ISENSE	53B1
SMC_PBUS_VSENSE	SMC_12V_S0_VSENSE	53B2
SMC_BATT_ISENSE	SMC_12V_S5_ISENSE	53B1
SMC_NB_MISC_ISENSE	SMC_12V_S5_VSENSE	53B4
SMS_X_AXIS	SMC_1V5_S0_VSENSE	54C3
SMS_Y_AXIS	SMC_MCP_CORE_VSENSE	54B4
SMC_NB_DDR_ISENSE	SMC_1V5_S0_ISENSE	54D3
SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	54B4

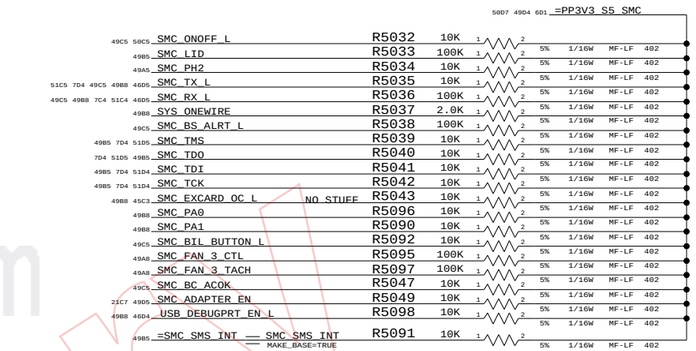
MISC. SIGNAL ALIASES

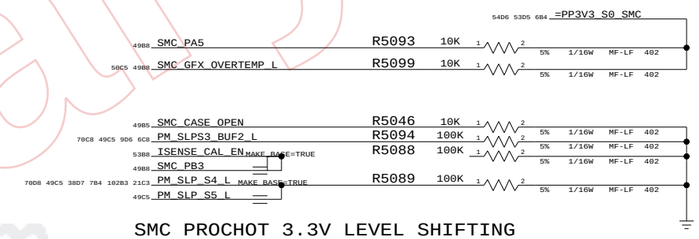
SMC_ANALOG_ID	ACDC_TEMP	6D6
SMC_GFX_OVERTEMP_L	MXM_ALERT_L	85B8
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	85B8



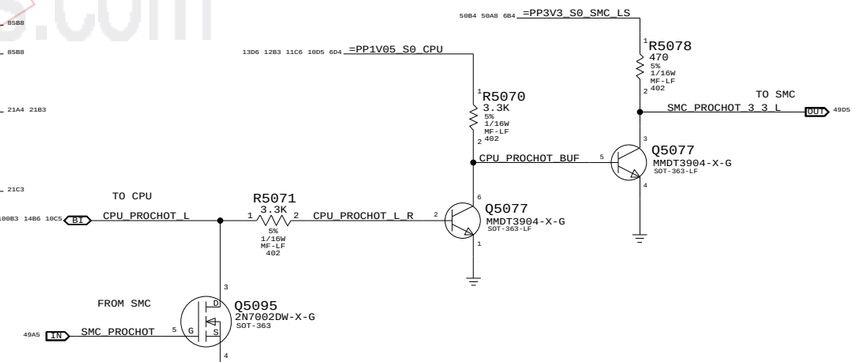
SIL: FOR DEVELOPMENT USE ONLY



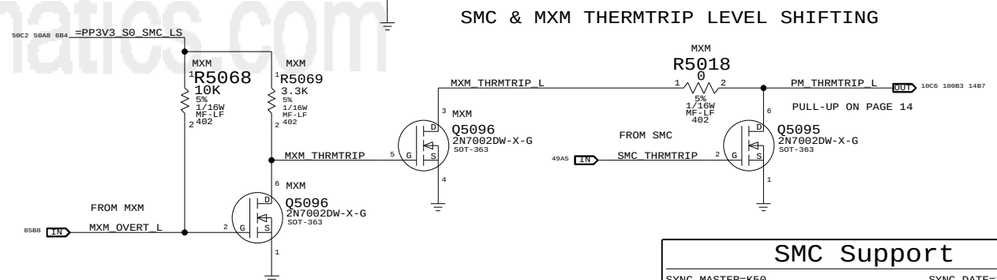




SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SMC Support

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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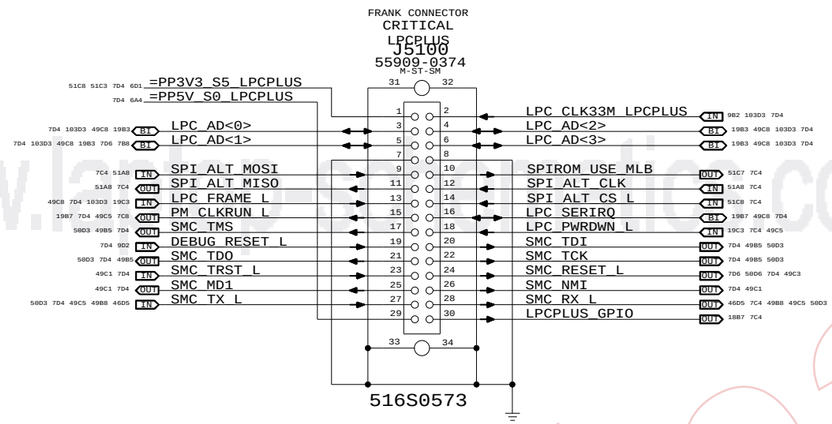
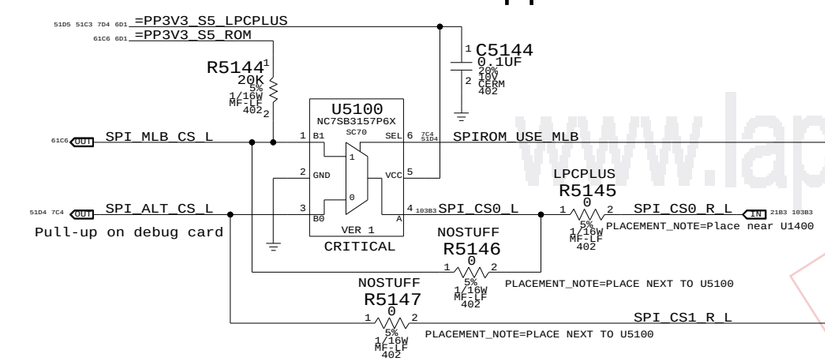
LPC+SPI Connector

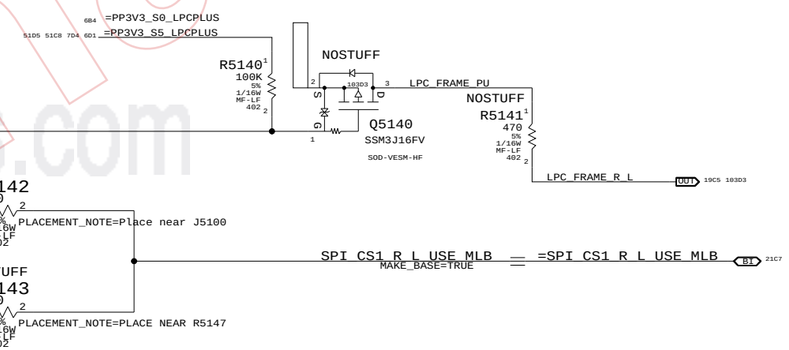


Alternate SPI ROM Support



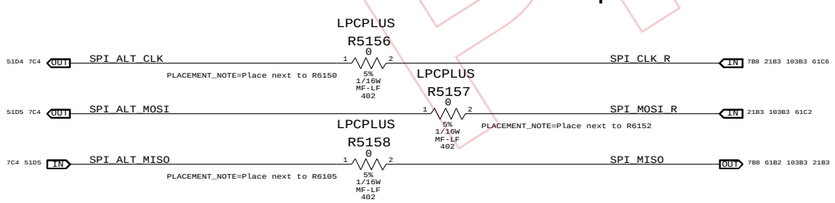
MCP79 Internal SPI MUX Support

Not supported in Rev A01 MCP79 silicon



MCP79 Rev A01 requires external MUX, Rev B01 should support internal MUX

SPI Bus Series Resistance Option



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LPC+SPI Debug Connector

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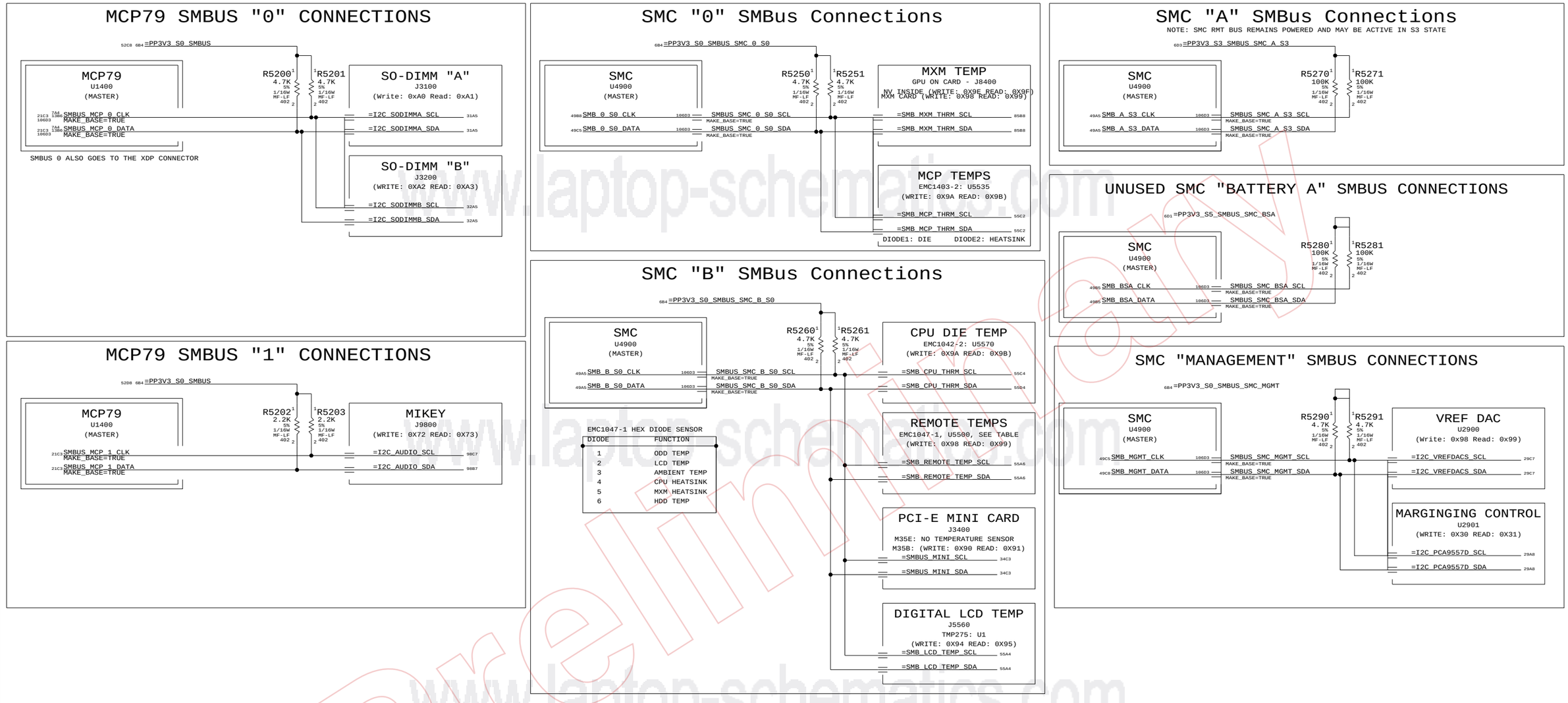
SCALE NONE	SHT 51 OF 109	



SMBUS CONNECTIONS

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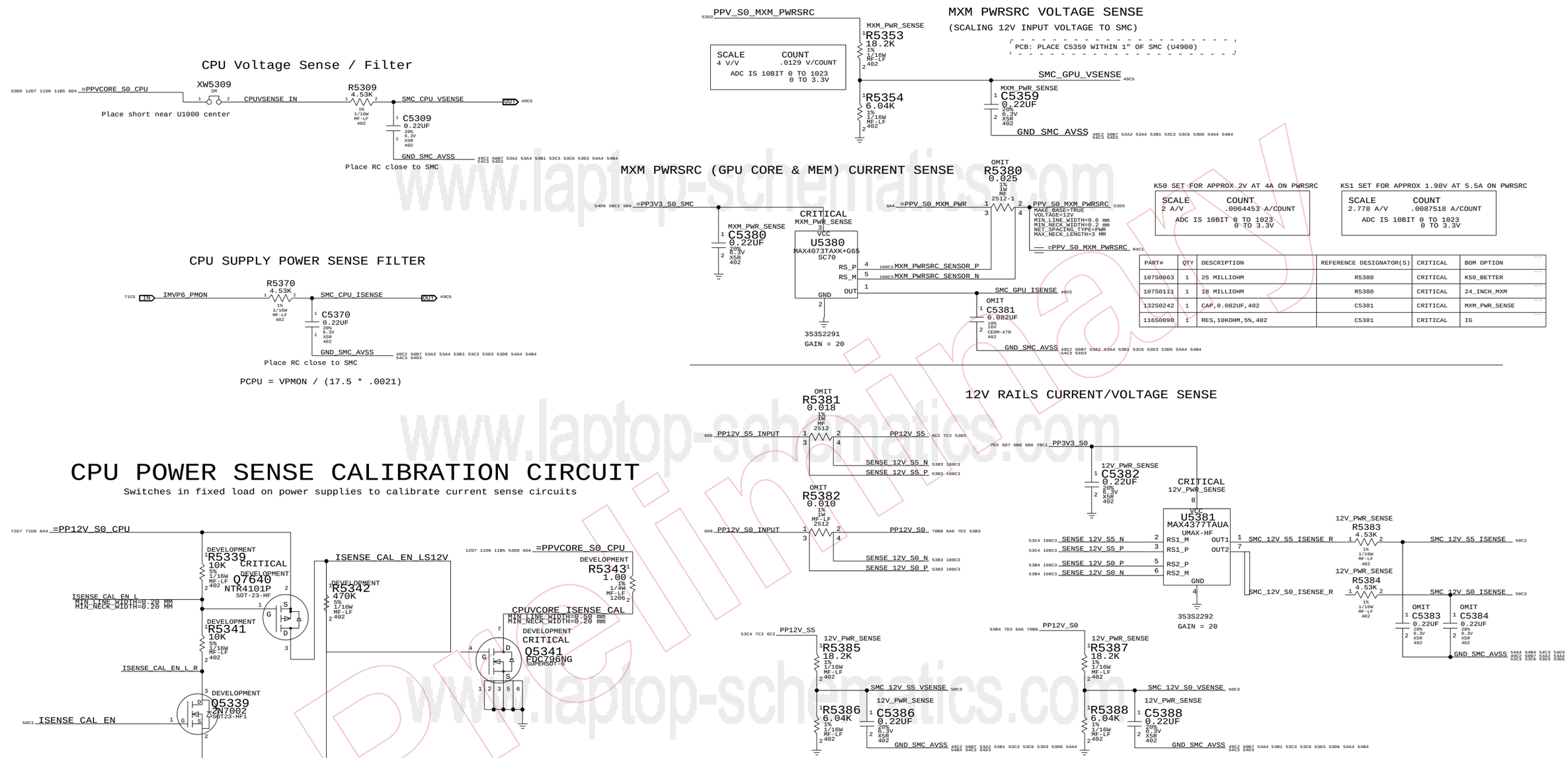

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K50_BETTER
107S0111	1	18 MILLIOHM	R5380	CRITICAL	24_INCH_MXM
132S0242	1	CAP,0.082UF,402	C5381	CRITICAL	MXM_PWR_SENSE
116S0090	1	RES,10KOHM,5%,402	C5381	CRITICAL	IG

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	RANGE
107S0069	1	10 MILLIOHM	R5382	CRITICAL	K50_BETTER	10A
107S0112	1	8 MILLIOHM	R5382	CRITICAL	24_INCH_MXM	12.5A
107S0070	2	RES,0 OHM,2512	R5381,R5382	CRITICAL	IG	
107S0111	1	18 MILLIOHM	R5381	CRITICAL	12V_PWR_SENSE	5.5A
116S0090	2	RES,10K0HM,5%,402	C5383,C5384		IG	
132S0080	2	CAP,0.22UF,20%,6.3V,X5R,402	C5383,C5384		12V_PWR_SENSE	

12V_PWR_SENSE SHOULD BE STUFFED FOR MXM CONFIGS
IG CONFIGS WILL NOT HAVE THE SENSORS, SO CAPS FROM THE RC FILTER BECOME RESISTORS TO GROUND (SO SMC READS 0)

IG CONFIGS DO NOT NEED 12V POWER SENSE BECAUSE THE CONFIGURATION DOES NOT DRAW CURRENT WHICH APPROACHES THE ACDC SPEC

Current & Voltage Sensing

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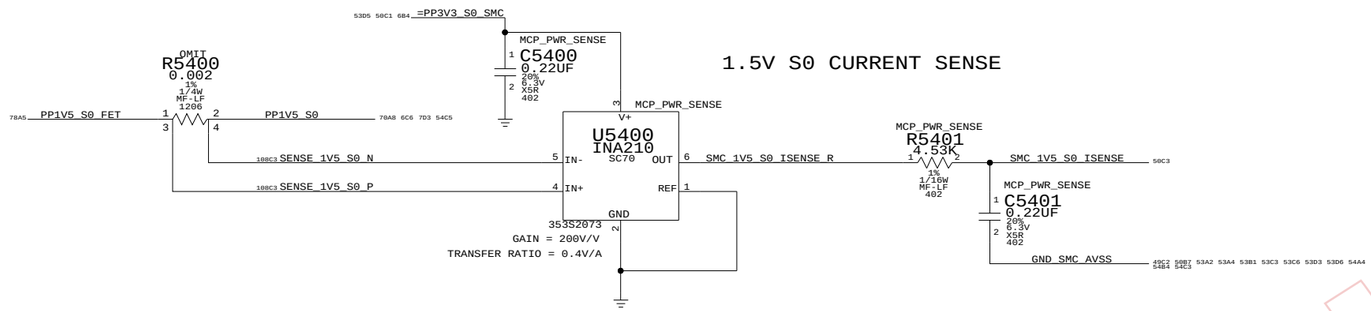
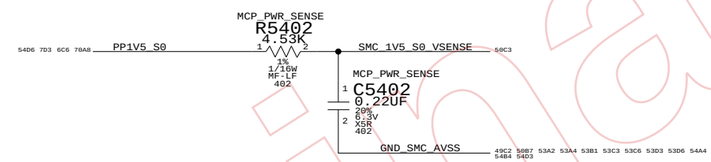
1.5V S0 CURRENT SENSE

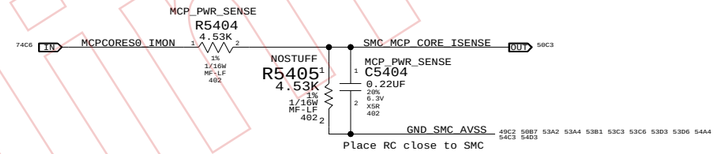


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

1.5V S0 VOLTAGE SENSE

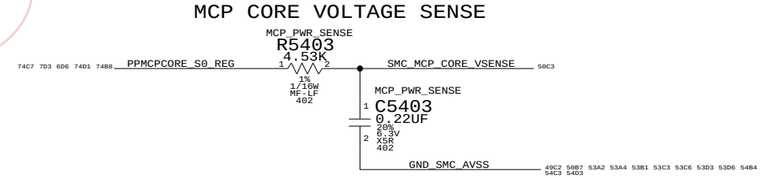


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



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MCP CURRENT AND VOLTAGE SENSE

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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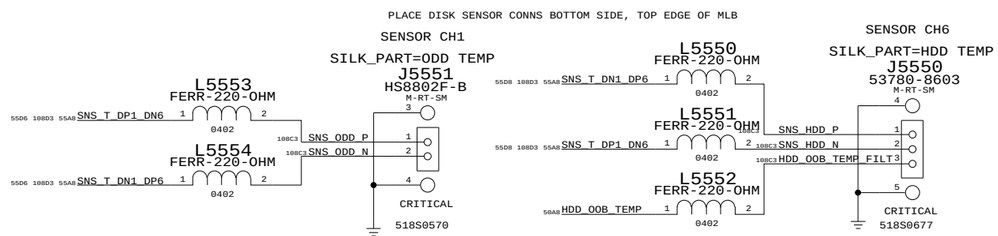
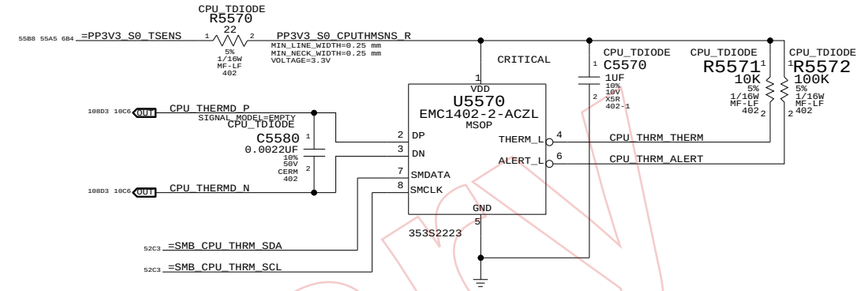
SHT 54 OF 109

REMOTE THERMAL SENSORS

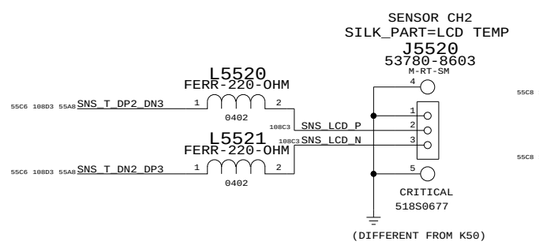
HEATSINKS, AMBIENT, PANEL AND DISKS



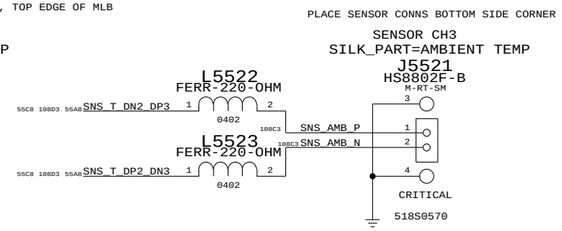
CPU T-Diode Thermal Sensor



PLACE ANALOG LCD TEMP CONN BOTTOM SIDE, TOP EDGE OF MLB

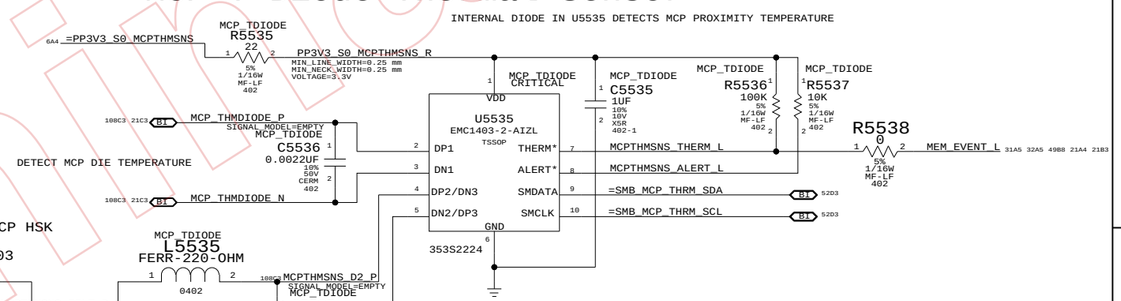


PLACE SENSOR CONNS BOTTOM SIDE CORNER

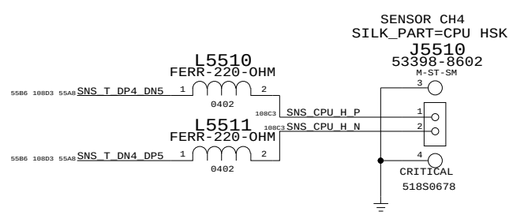


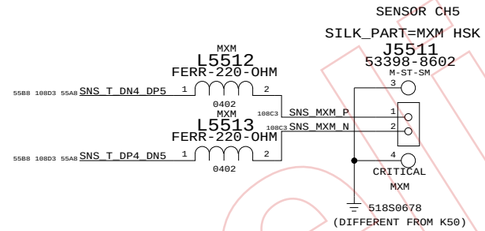
MCP T-Diode Thermal Sensor

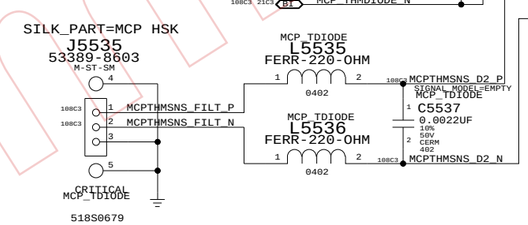
INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE



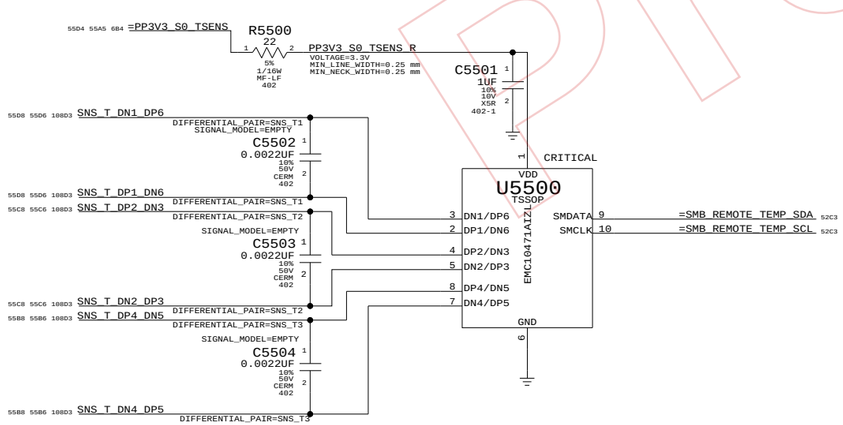
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU





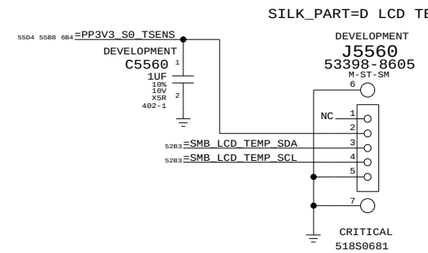


REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)



DIGITAL LCD TEMP SENSOR

SILK_PART=D LCD TEMP



BROKE SYNC FROM K50 ON 7/9

Thermal Sensors

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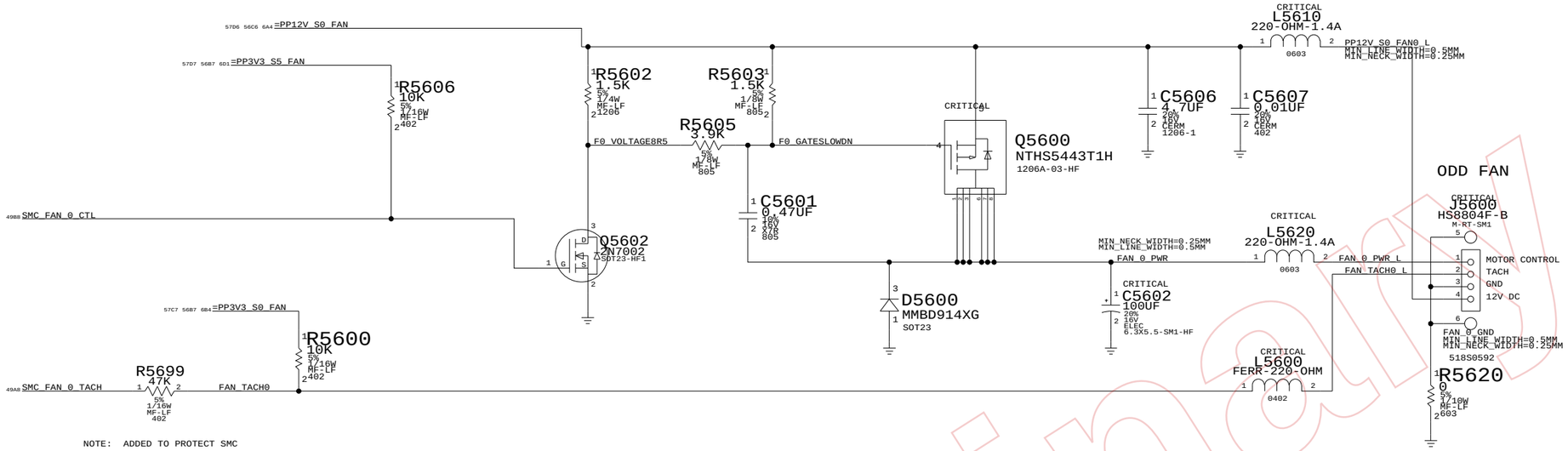
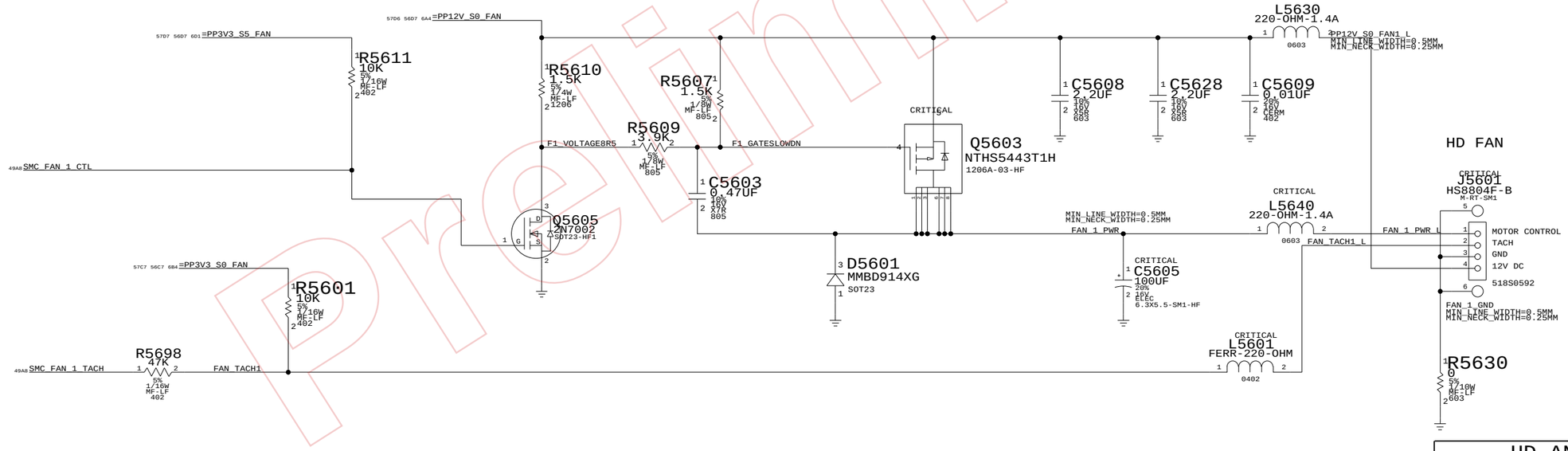
FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



Preliminary

HD AND OD FAN

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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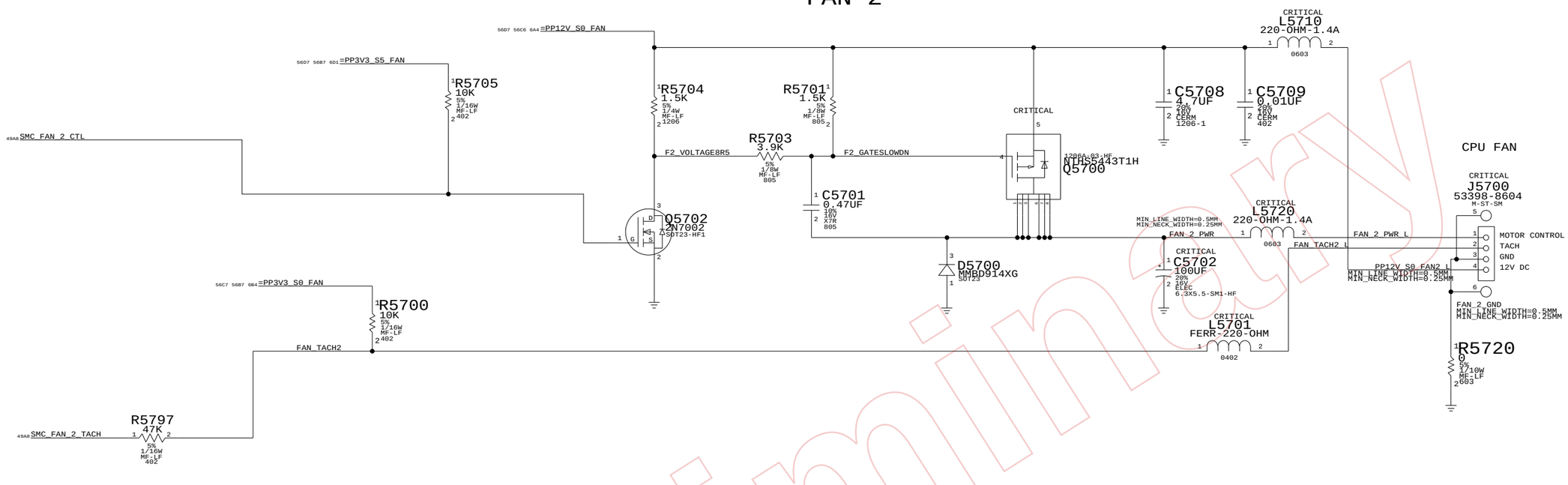
FAN 2



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CPU FAN

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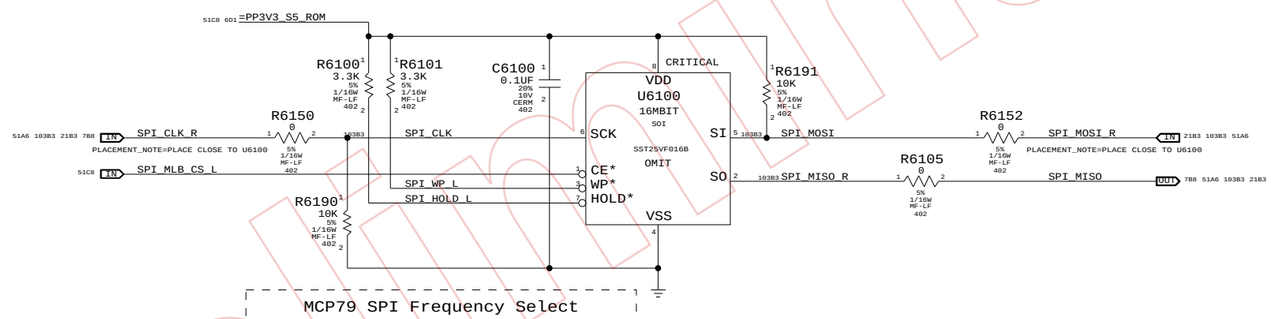
SCALE NONE	SHT 57 OF 109	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

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SPI ROM

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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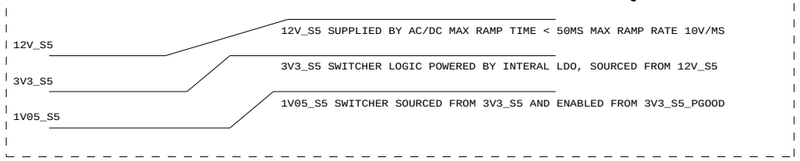
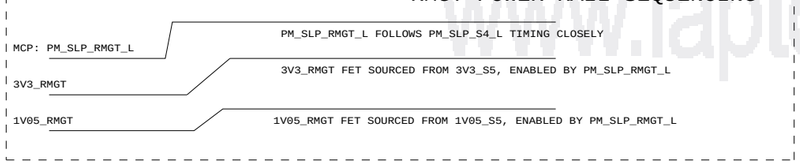
SCALE NONE	SHT 61 OF 109	

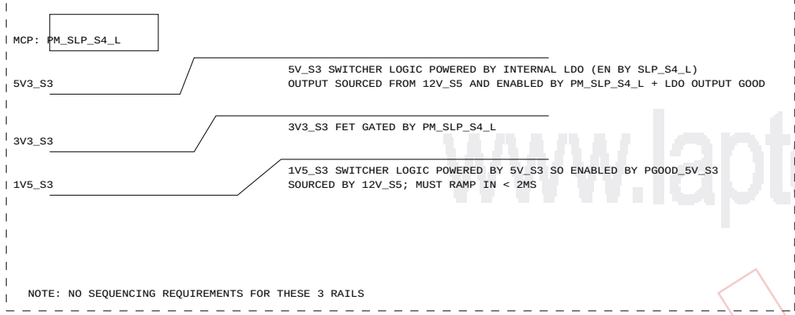
S5 POWER RAIL SEQUENCING



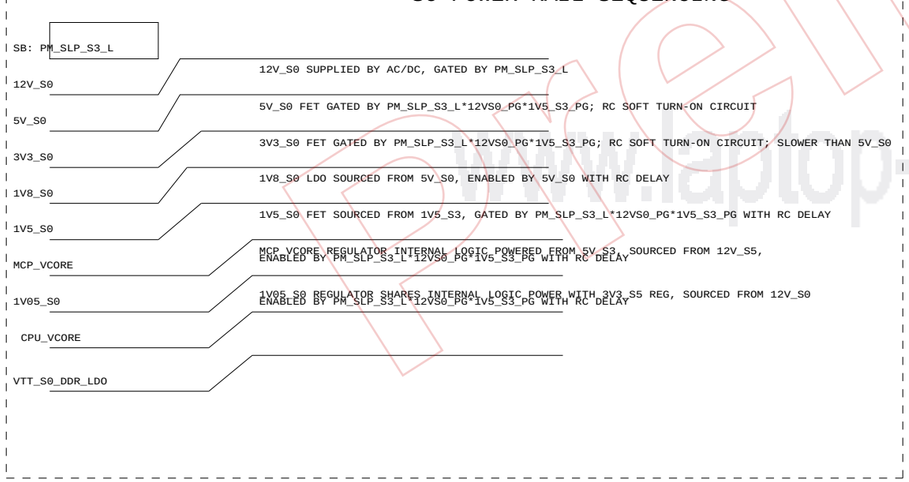
RMGT POWER RAIL SEQUENCING



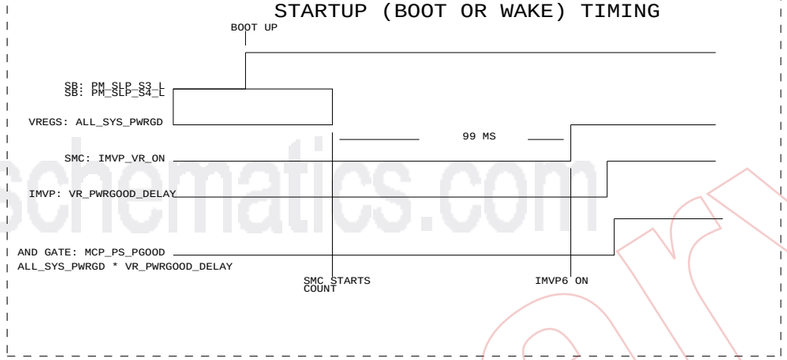
S3 POWER RAIL SEQUENCING



S0 POWER RAIL SEQUENCING



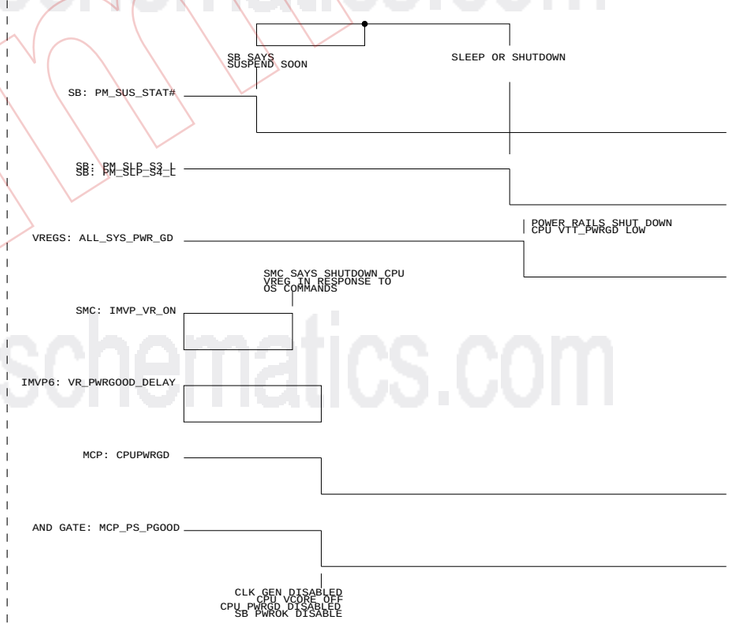
STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING

POWER RAILS ON DURING THIS TIME



POWER SEQUENCING BLOCK DIAGRAM

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State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Power Control Signals

3.3V,5V S3 enable

FROM MCP (6)

50C3 49C5 38D7 7B4 102B3 21C3 IN PM_SLP_S4_L (PM_S4_STATE_L) MAKE_BASE=TRUE

=P3V3S3_EN OUT 78D4 Enable FET

=5VREG_EN OUT 73C6 ENABLE REGULATOR

MXM POWER SEQUENCE

85B2 IN =PM_MXM_PGOOD_PULLUP — ALL_SYS_PWRGD_R 70B1 6B7 7B4 7C3 7C4 MAKE_BASE=TRUE — PM_MXM_EN OUT 85B8

MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

78B7 6C9 =PP5V_S3_PWRCTL — R7072 100K 5% 1/16W MF-LF 402

9A7 PGOOD_5V_S3 MAKE_BASE=TRUE

=DDRREG_EN OUT 75C8 Enable regulator

70C1 70B3 70B1 70A3 6D1 =PP3V3_S5_PWRCTL — C7058 0.1UF 20% 10V CERM 402

R7040 100K 5% 1/16W MF-LF 402

FROM COMPARATOR
70B4 PGOOD_1V5_S3
FROM COMPARATOR
70B4 PGOOD_12V_S0

S0_RDY MAKE_BASE=TRUE

U7059 TC7SZ08AFEAPE SOT665

49C5 9D6 6C8 50C3 IN PM_SLPS3_BUF2_L (PM_SLP_S3_L) — From SMC (6)

4 (PM_SLP_S3_L_BUF) — PM_SLP_S3_L_AND_S0_RDY MAKE_BASE=TRUE

=P5VS0_EN OUT 78D7 Enable FET

=P3V3S0_EN OUT 78C4 Enable FET

R7080 30K 5% 1/16W MF-LF 402 — R7081 43K 5% 1/16W MF-LF 402 — R7082 10K 5% 1/16W MF-LF 402

MCPDDR_EN MAKE_BASE=TRUE — =MCPDDR_EN OUT 78A7 Enable FET DELAY OF ~15MS FROM PM_SLP_S3_L

CPUVTTS0_EN MAKE_BASE=TRUE — =1V05S0_EN OUT 76B7 Enable regulator DELAY OF ~18MS FROM PM_SLP_S3_L

MCPCORES0_EN MAKE_BASE=TRUE — =MCPCORES0_EN OUT 74C6 Enable regulator DELAY OF ~16MS FROM PM_SLP_S3_L

C7080 0.47UF 10% 6.3V CERM-X5R 402 — C7081 0.47UF 10% 6.3V CERM-X5R 402 — C7082 0.47UF 10% 6.3V CERM-X5R 402

1.5V_S3 NEED TO BE ON BEFORE S0 FET ON
12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN

=PP3V3_S5_PWRCTL 6D1 70A3 70B1 70B3 70D8 — R7031 1K 5% 1/16W MF-LF 402

79B4 PGOOD_1V05_S5 — 1V05V_S0 DERIVES FROM 3.3V_S5

RSMRST_PWRGD OUT 49D8 To SMC (2)

C7031 0.1UF 10% 16V X5R 402 — FROM THIS SMC GENERATES PM_RSMRST_L WHICH GOES INTO PGOOD_S8 OF MCP DELAY IS ABOUT 200MS

PGOOD Comparators

6C1 =PP12V_S5_PWRCTL

R7013 33.2K 1% 1/16W MF-LF 402 — R7018 84.5K 1% 1/16W MF-LF 402 — IG R7020 64.9K 1% 1/16W MF-LF 402

C7010 0.1UF 20% 16V CERM 603

XW7000 — 7D3 6A6 5384 6385 PP12V_S0 — OMIT SM — R7000 4.99K 1% 1/16W MF-LF 402 — 12VS0_PG_CMP

XW7001 — 6D3 =PPDDR_S3_PGCMP — OMIT SM — 1V5S3_PG_CMP — R7001 1.21K 1% 1/16W MF-LF 402

USING COMPARTOR INSTEAD OF REGULATOR
PGOOD OUTPUT BECAUSE IF 5V_S3 GOES
NOT COME UP, PCDDR REGULATOR HAS
NO INTERNAL POWER TO PULL PGOOD
LOW

IG R7002 2.0K 1% 1/16W MF-LF 402

6C4 =PP1V8_S0_PGCMP — XW7002 — OMIT SM — 1V8S0_PG_CMP

6A6 7B9 7D3 PP5V_S0 — XW7003 — OMIT SM — 5VS0_PG_CMP — MXM R7004 4.7K 1% 1/16W MF-LF 402

1V5S0_PG_CMP — R7003 1.21K 1% 1/16W MF-LF 402

54C5 7D3 6C9 5406 PP1V5_S0 — XW7004 — OMIT SM

PLACE SHORTS CLOSE TO PLANE CUTS

(9.91V/9.58V; 330MV HYSTERESIS)

(1.30V/1.22V; 80MV HYSTERESIS)

1V60 IF 1.8V CMP (1.67V/1.53V; 132MV HYSTERESIS)

4V12 IF 5V CMP (4.51V/4.20V; 310MV HYSTERESIS)

(1.30V/1.22V; 80MV HYSTERESIS)

R7014 100K 1% 1/16W MF-LF 402 — R7019 10K 1% 1/16W MF-LF 402 — R7021 10K 1% 1/16W MF-LF 402

CRITICAL

U7010 LM339A SOI-HF

12VS5_9V00_REF	-1	OUT1
12VS0_COMP_REF	+1	
(12VS5_1V27_REF)	-2	OUT2
1V5S3_COMP_REF	+2	
12VS5_1V60_REF	-3	OUT3
1V8S0_COMP_REF	+3	
12VS5_1V27_REF	-4	OUT4
1V5S0_COMP_REF	+4	
		GND

R7005 49.9K 1% 1/16W MF-LF 402 — R7006 49.9K 1% 1/16W MF-LF 402 — R7007 49.9K 1% 1/16W MF-LF 402 — R7008 49.9K 1% 1/16W MF-LF 402

PGOOD_12V_S0 OUT 70C8

PGOOD_1V5_S3 OUT 70C8

PGOOD_1V8S0_OR_5VS0 OUT 70B4

PGOOD_1V5_S0 OUT 70B4

(PULLUPS ARE NEAR LOADS)

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0341	1	RES,19.1K,1%,402	R7020		MXM

S0 RAILS PGOOD

70D8 70C1 70B1 70A3 6D1 =PP3V3_S5_PWRCTL — R7033 10K 1% 1/16W MF-LF 402

70B4 PGOOD_1V8S0_OR_5VS0

70A4 PGOOD_1V5_S0

CAN I USE ALIAS OR DO I NEED INLINE RESISTOR?

=PP3V3_S5_PWRCTL 6D1 70A3 70B3 70C1 70D8 — C7020 0.1UF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO U7020

6B4 =PP3V3_S0_PWRCTL — R7030 10K 5% 1/16W MF-LF 402

74C6 IN PGOOD_MCPCORE_S0

76B3 IN PGOOD_1V05_S0

S0_PWR_CMP_PGOOD MAKE_BASE=TRUE

S0_PWR_REG_PGOOD MAKE_BASE=TRUE

U7020 TC7SZ08AFEAPE SOT665

4 ALL_SYS_PWRGD

R7098 33 5% 1/16W MF-LF 402 — ALL_SYS_PWRGD_SMC OUT 49D8

R7099 33 5% 1/16W MF-LF 402 — ALL_SYS_PWRGD_R OUT 70D3 6B7 7B4 7C3 7C4

	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

70D8 70C1 70B3 70B1 6D1 =PP3V3_S5_PWRCTL — C7056 0.1uF 20% 10V CERM 402

85B3 85B8 IN PM_MXM_PGOOD

7C4 71C7 7C7 IN VR_PWRGOOD_DELAY

U7056 MC74VHC1G08 SOT23-5-HF

MCP_PS_PWRGD OUT 21B7

ALL_SYS_PWRGD IS ALSO AN INPUT TO THIS AND GATE BY THE FACT THAT PM_MXM_PGOOD IS PULLED UP TO IT

PGOOD and Power Sequencing

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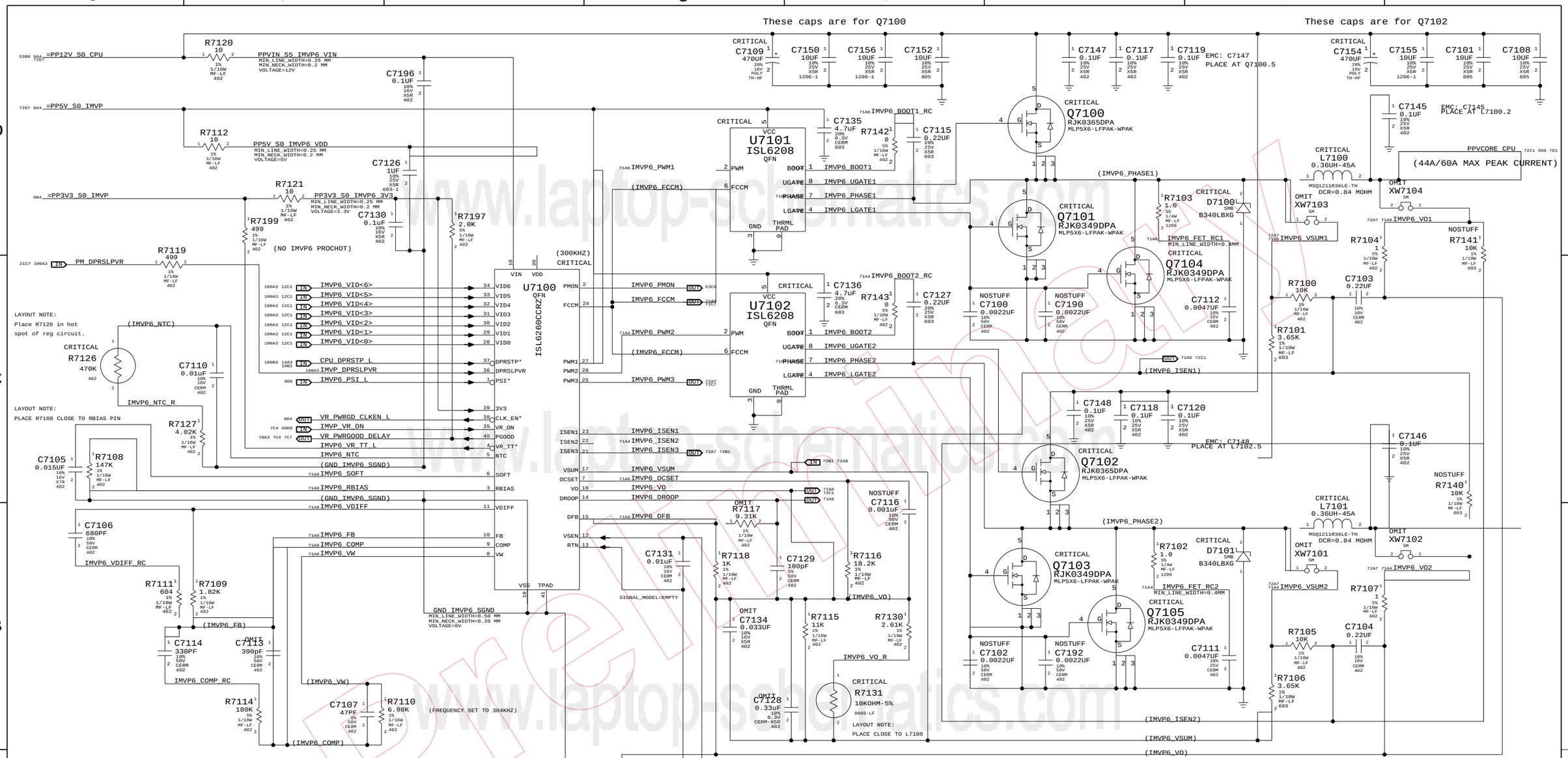

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

- 55W PENRYN MODT PROCESSORS: 68A CONTINUOUS CURRENT
  SET R7116 TO 18.2K; OC TRIP POINT OF 86.8A, WORST CASE MIN OF 76A.

71C5	IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71C4 72B1	IMVP6_VSUM	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
72C1 71C4	IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71C4	IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71B5	IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71C7	IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71C7	IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71B7	IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71B7	IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71B7	IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
71B7	IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
72C7 71C5	IMVP6_FCCM	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM

71D5	IMVP6_PWM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM
108D3 71D4	IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM
71D4	IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
71D4	IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM
71D4	IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM
72C1 71C3	IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM
71D3	IMVP6_FET_RC1	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM
72A7 71D2	IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
72A7 71D1	IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
71D4	IMVP6_BOOT1_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM

71C5	IMVP6_PWM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM
108D3 71C4	IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM
71C4	IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
71C4	IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM
71C4	IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM
71C5	IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM
71B9	IMVP6_FET_RC2	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM
72A7 71B2	IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
72A7 71B1	IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
71C4	IMVP6_BOOT2_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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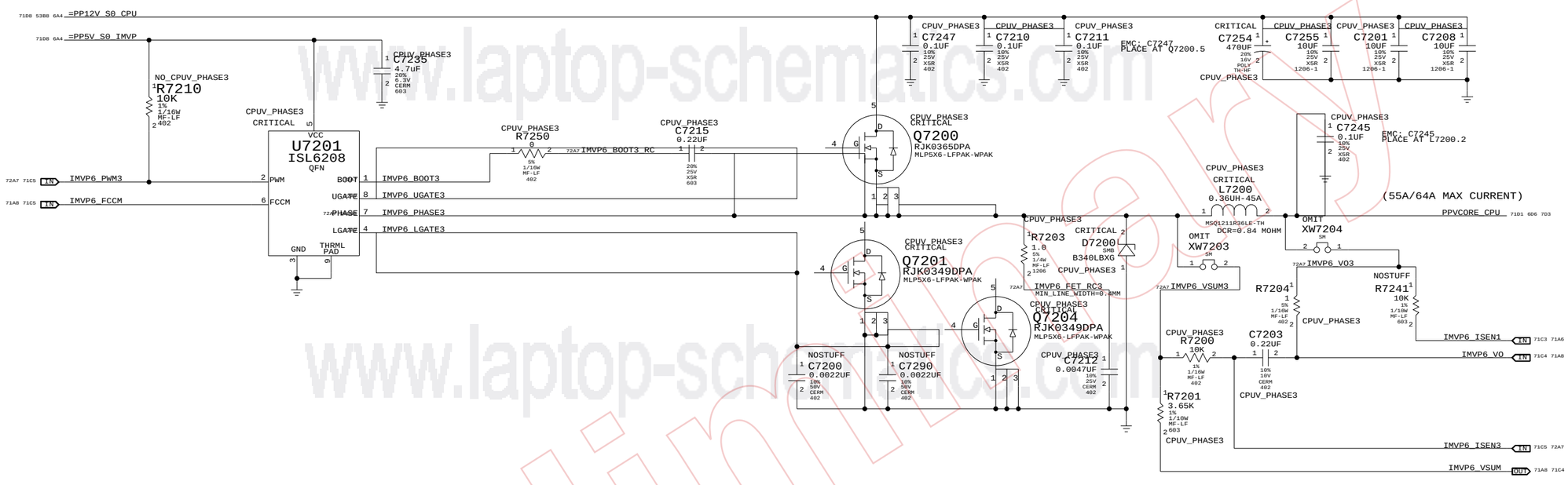
IMVP6 CPU VCORE REGULATOR



NO TEST FOR CPU VREG, ADDED K2/K3

IMVP6_VO1	NO_TEST=TRUE	
IMVP6_VO2	NO_TEST=TRUE	
IMVP6_VO3	NO_TEST=TRUE	
IMVP6_VSUM1	NO_TEST=TRUE	
IMVP6_VSUM2	NO_TEST=TRUE	
IMVP6_VSUM3	NO_TEST=TRUE	

IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	T51
IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	T43
IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T44
IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	T45
IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	T46
IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	T48
IMVP6_FET_RC3	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM	T47
IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T49
IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T50
IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	T57

IMVP6 3RD PHASE

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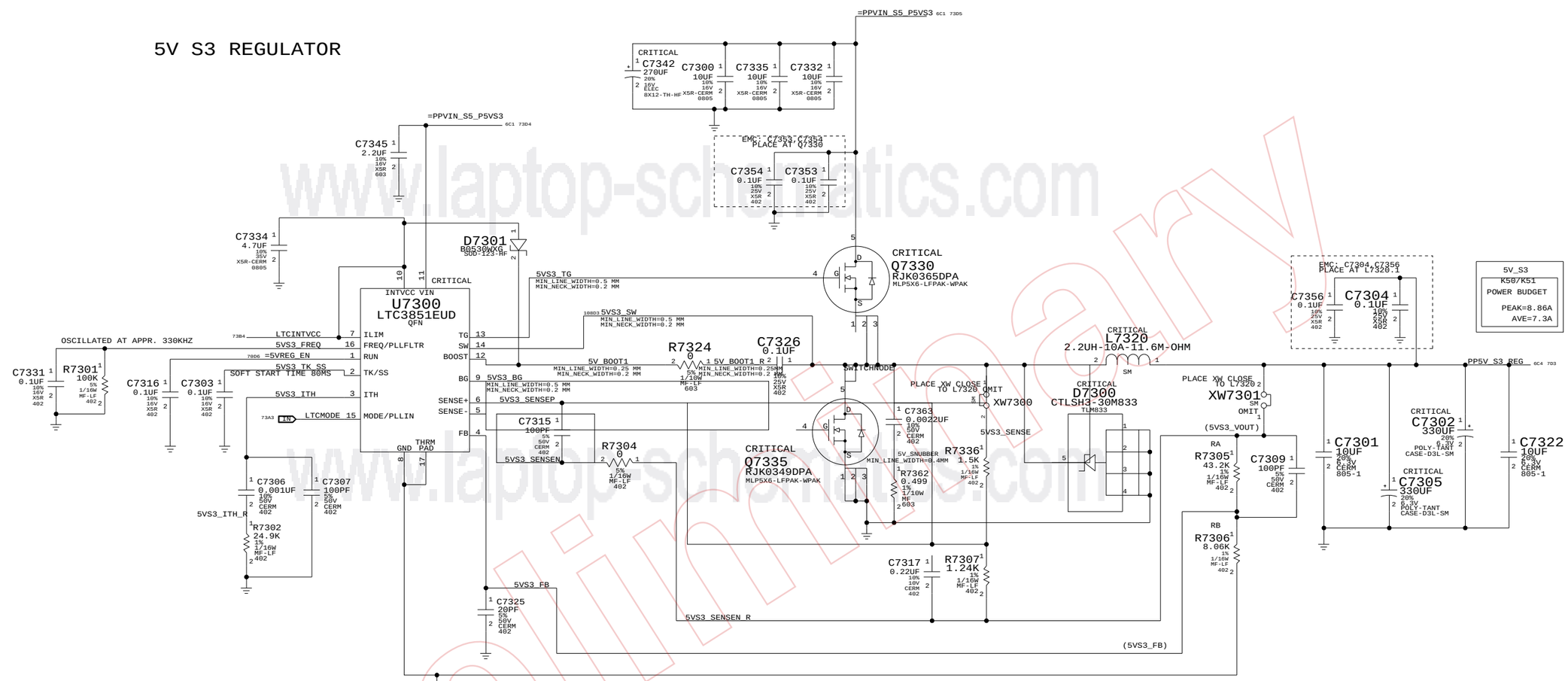
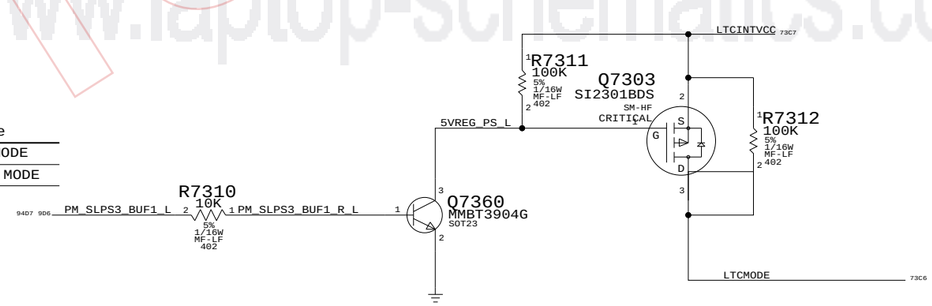
5V S3 REGULATOR





STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

5V_S3 REGULATOR

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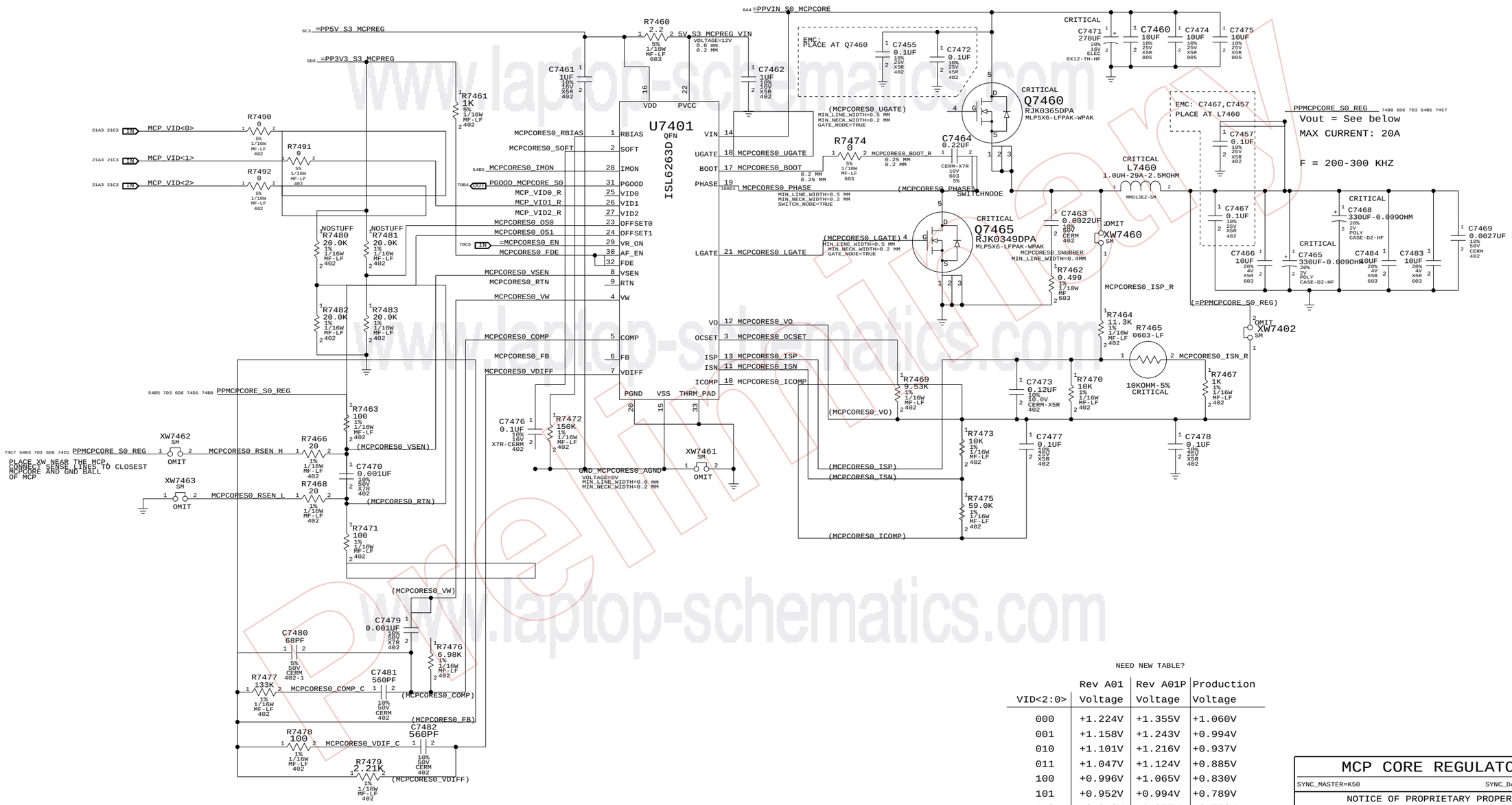
MCP CORE



NEED NEW TABLE?

VID<2:0>	Rev A01 Voltage	Rev A01P Voltage	Production Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

MCP CORE REGULATOR

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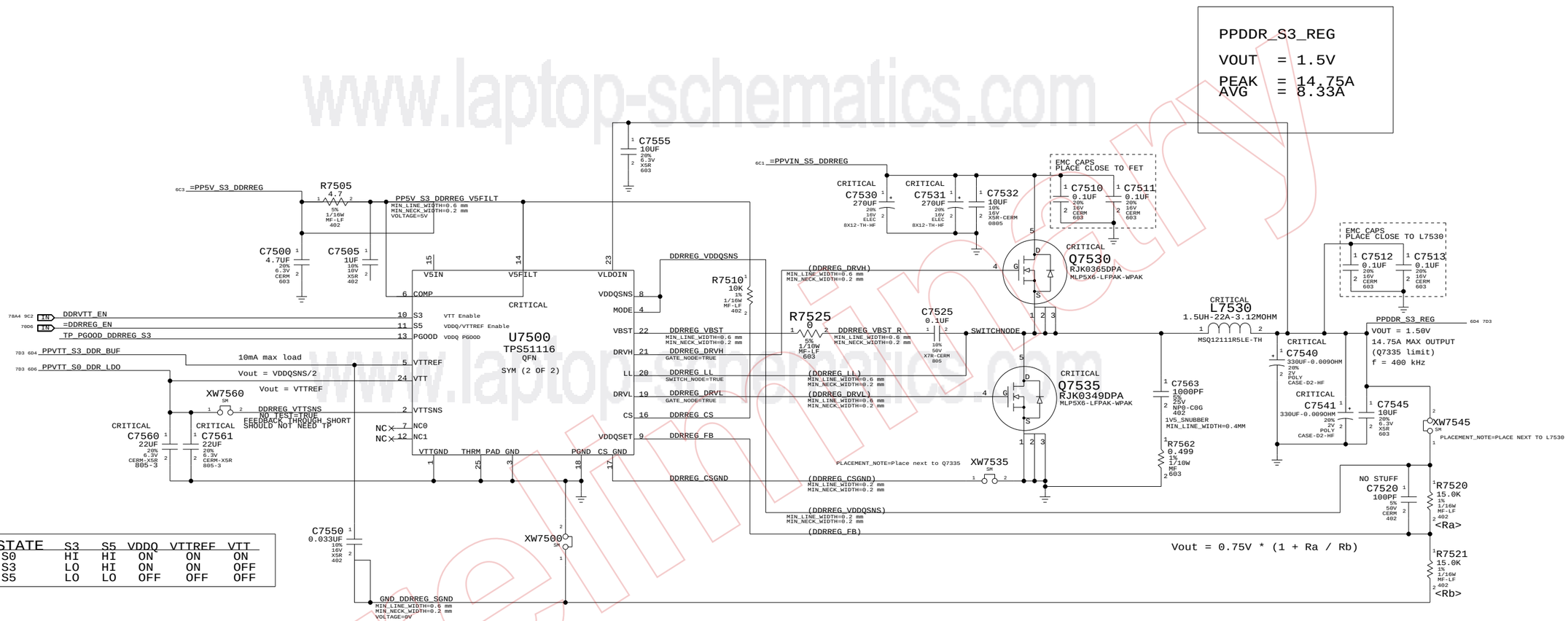
1.5 V DDR SUPPLY



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

1.5V DDR SUPPLY

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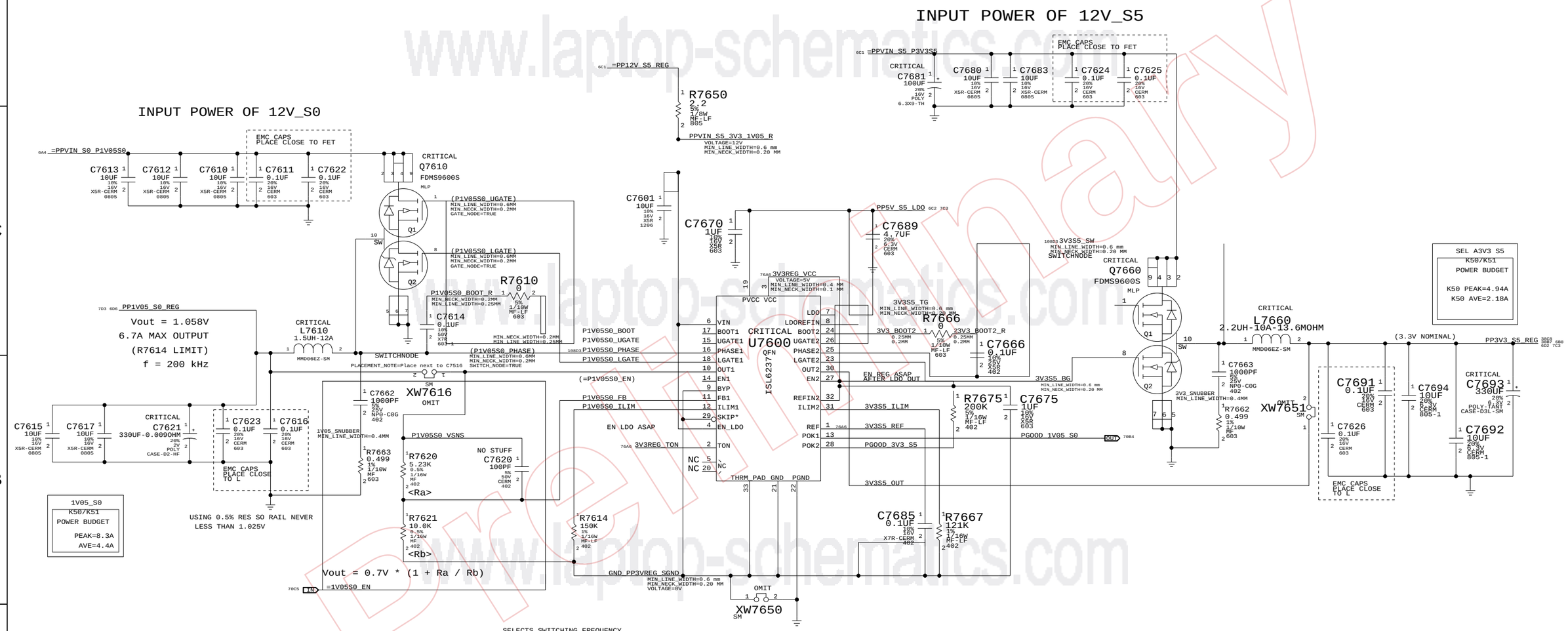
3.3V S5 AND 1.05 S0 RAILS



EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT. SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (1.05_S0) CONTROLLED SEPARATELY

1.05VS0/3.3V S5 SUPPLIES

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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D	051-7840	10

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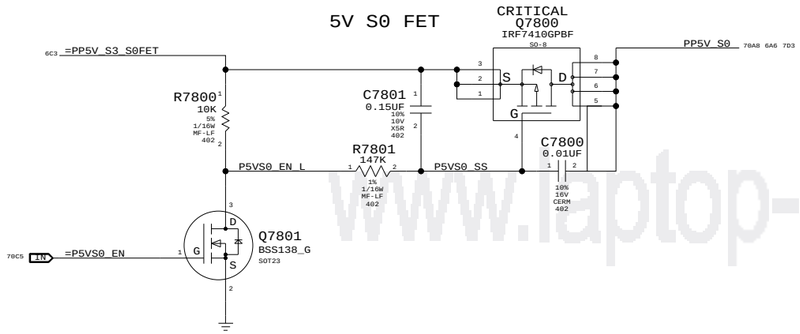
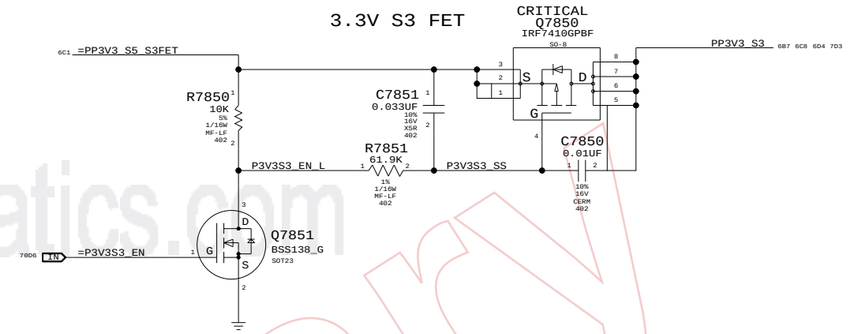
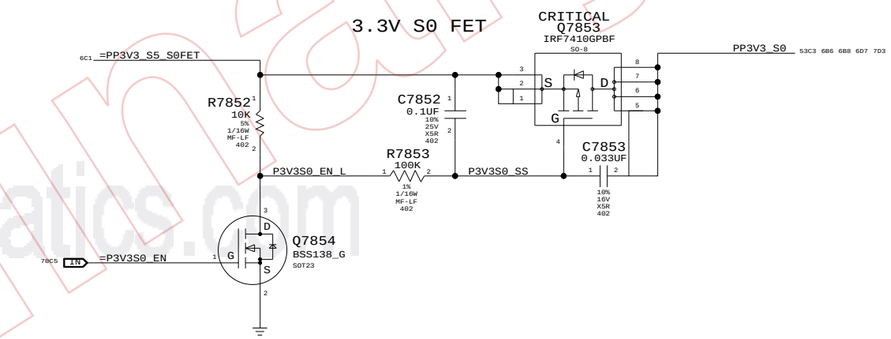
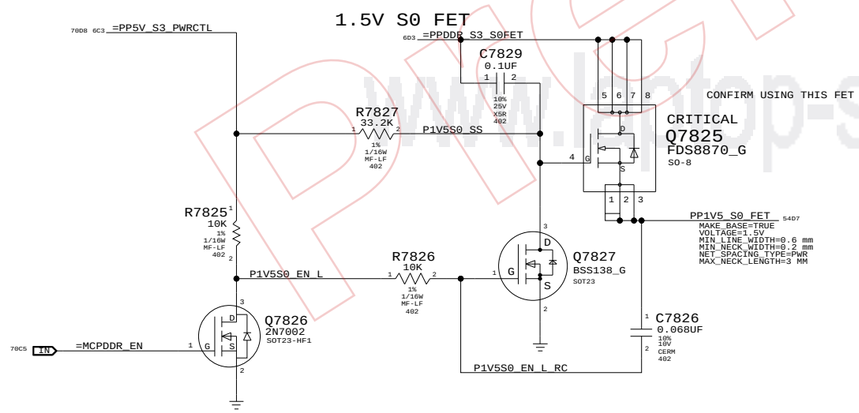


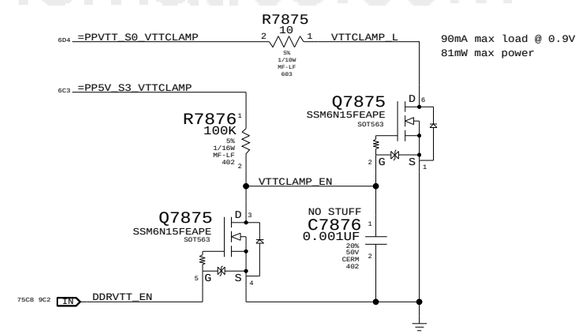






MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

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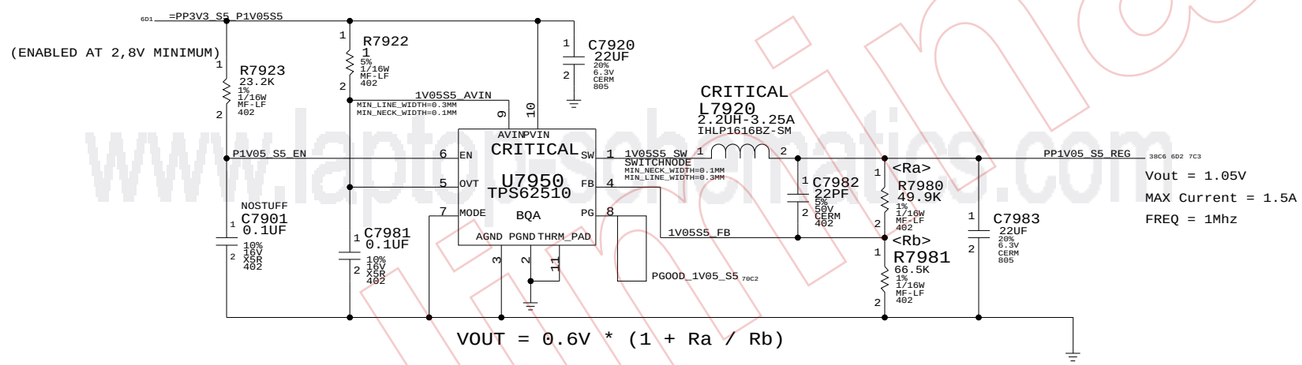
MCP 1.05V_S5 AUXC SUPPLY



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1V05 S5 POWER SUPPLY

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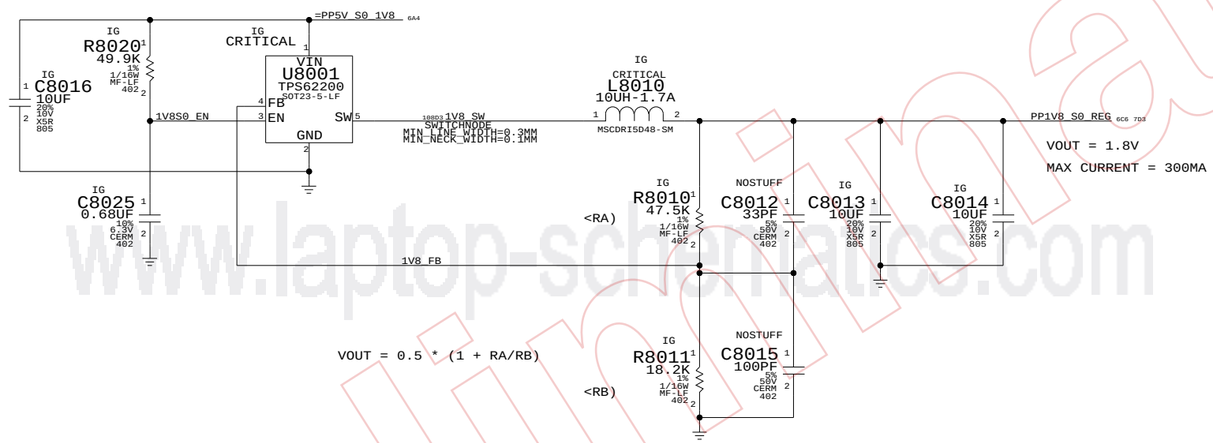
MCP ONLY 1.8V_S0 POWER SUPPLY



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1V8 POWER SUPPLY

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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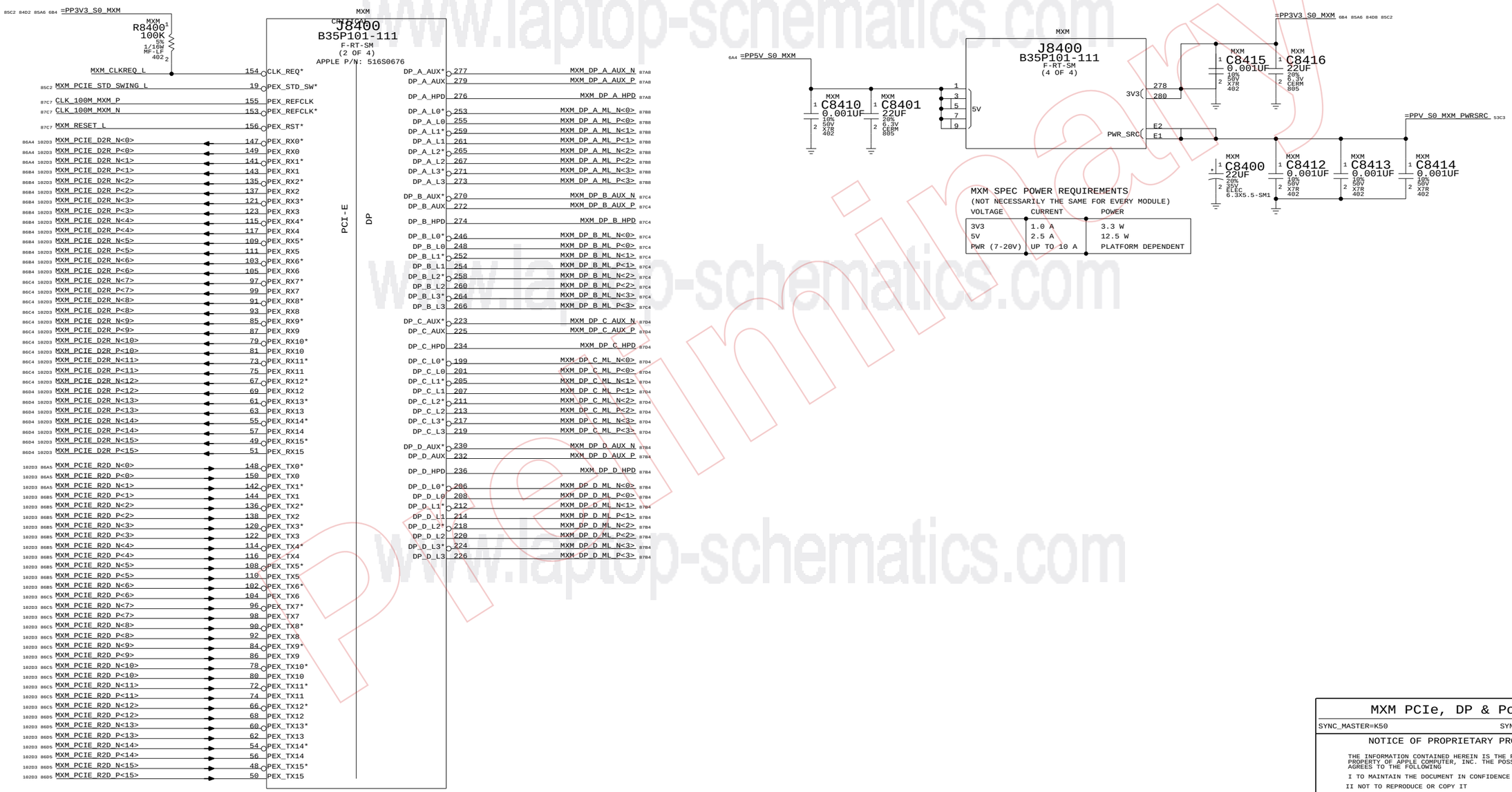
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

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MXM PCIe, DP & Power

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SIZE	DRAWING NUMBER	REV.
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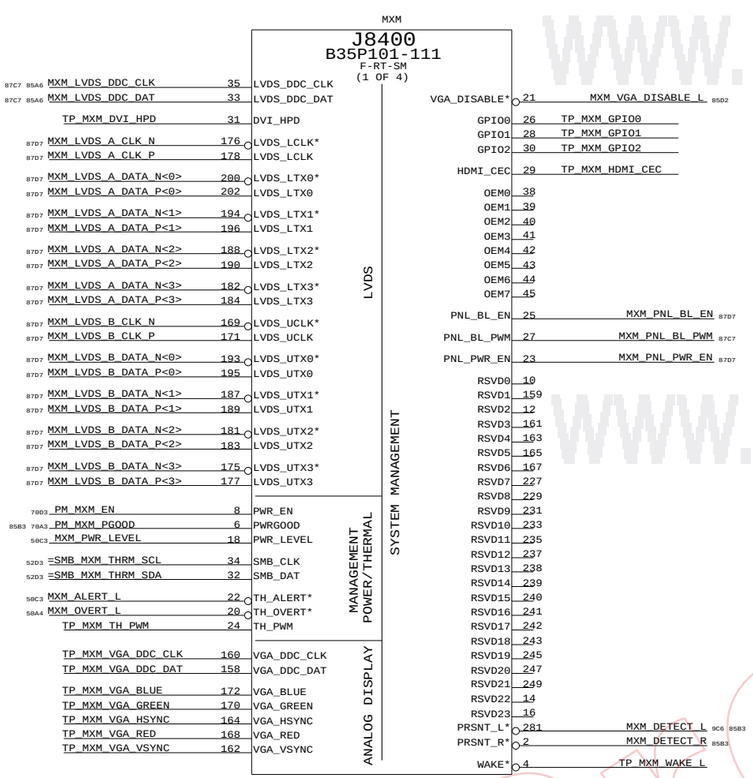
Page Notes

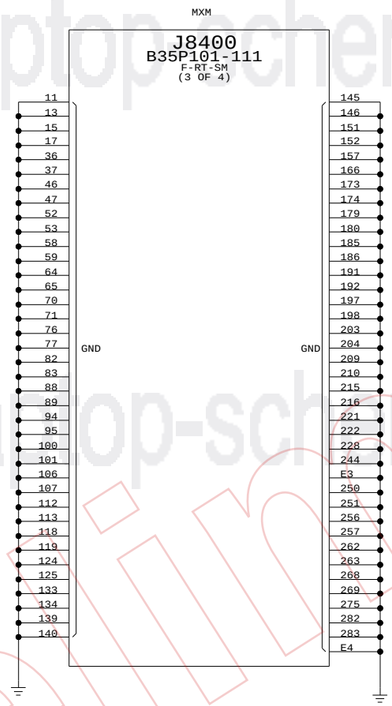
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR





ELOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

ELOAT = LOW SWING
GND = HIGH SWING

MXM_VGA_DISABLE_L — R8510 0 MF-LF 5% 1/16W 402 NOSTUFF

MXM_PCIE_STD_SWING_L — R8504 0 MF-LF 5% 1/16W 402 MXM

=PP3V3_S0_MXM

MXM_DETECT_L — R8500 100K MF-LF 5% 1/16W 402

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

MXM_DETECT_R — R8501 100K MF-LF 5% 1/16W 402

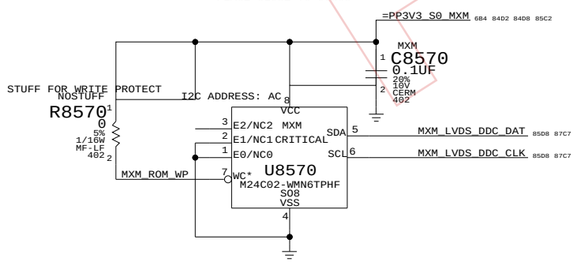
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

PM_MXM_PGOOD — R8503 10K MF-LF 5% 1/16W 402

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



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MXM I/O

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SLOTB MXM TX CAPS

102D3 9C6	IN	PEG_R2D_C_N<0>	MXM	C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_P<0>	MXM	C8601	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_P<1>	MXM	C8602	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_N<1>	MXM	C8603	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_N<2>	MXM	C8604	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_P<2>	MXM	C8605	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_N<3>	MXM	C8606	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_P<3>	MXM	C8607	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_N<4>	MXM	C8608	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_P<4>	MXM	C8609	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_N<5>	MXM	C8610	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_P<5>	MXM	C8611	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	OUT	102D3 84A8
102D3 9C6	IN	PEG_R2D_C_N<6>	MXM	C8612	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>	OUT	102D3 84A8
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102D3 9C6	IN	PEG_R2D_C_N<7>	MXM	C8614	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	OUT	102D3 84A8
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102D3 9C6	IN	PEG_R2D_C_P<12>	MXM	C8625	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>	OUT	102D3 84B8
102D3 9C6	IN	PEG_R2D_C_N<13>	MXM	C8626	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>	OUT	102D3 84B8
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102D3 9C6	IN	PEG_R2D_C_N<14>	MXM	C8628	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>	OUT	102D3 84B8
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102D3 9C6	IN	PEG_R2D_C_N<15>	MXM	C8630	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>	OUT	102D3 84B8
102D3 9C6	IN	PEG_R2D_C_P<15>	MXM	C8631	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	OUT	102D3 84B8

SLOTB MXM RX CAPS

102D3 84B8	IN	MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<0>	OUT	102D3 9C6
102D3 84B8	IN	MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT	102D3 9C6
102D3 84B8	IN	MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT	102D3 9C6
102D3 84B8	IN	MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT	102D3 9C6
102D3 84B8	IN	MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT	102D3 9C6
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102D3 84B8	IN	MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<4>	OUT	102D3 9C6
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102D3 84C8	IN	MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<6>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<7>	OUT	787 102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<8>	MXM	C8647	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<7>	OUT	787 102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<8>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<9>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<9>	OUT	102D3 9C6
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102D3 84C8	IN	MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT	102D3 9C6
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102D3 84C8	IN	MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT	102D3 9C6
102D3 84C8	IN	MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT	102D3 9C6

MXM PCIE CAPS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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Page Notes

Power aliases required by this page:
- =PP5V_DP_AUX

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

85C8	MXM_LVDS_A_DATA_P<3..0>	LVDS_EG_A_DATA_P<3..0> (MAKE_BASE=TRUE)	107C2 89B6 89C6 89D6 90A6 90A8
85C8	MXM_LVDS_A_DATA_N<3..0>	LVDS_EG_A_DATA_N<3..0> (MAKE_BASE=TRUE)	107C2 89B6 89C6 89D6 90A6 90A8
85C8	MXM_LVDS_B_DATA_P<3..0>	LVDS_EG_B_DATA_P<3..0> (MAKE_BASE=TRUE)	107C2 89A6 89C3 89D3 90A8 90B6
85C8	MXM_LVDS_B_DATA_N<3..0>	LVDS_EG_B_DATA_N<3..0> (MAKE_BASE=TRUE)	107C2 89A6 89C3 89D3 90A6 90B8
85C8	MXM_LVDS_A_CLK_N	LVDS_EG_A_CLK_N (MAKE_BASE=TRUE)	89B6 107C2
85C8	MXM_LVDS_A_CLK_P	LVDS_EG_A_CLK_P (MAKE_BASE=TRUE)	89B6 107C2
85C8	MXM_LVDS_B_CLK_N	LVDS_EG_B_CLK_N (MAKE_BASE=TRUE)	89C3 107C2
85C8	MXM_LVDS_B_CLK_P	LVDS_EG_B_CLK_P (MAKE_BASE=TRUE)	89C3 107C2
85C6	MXM_PNL_BL_EN	LVDS_BKL_ON (MAKE_BASE=TRUE)	6D6 8D3 90A3 90C4
85C6	MXM_PNL_PWR_EN	LVDS_EG_PANEL_PWR (MAKE_BASE=TRUE)	90A3 90B8
85C6	MXM_PNL_BL_PWM	LVDS_EG_BKL_PWM (MAKE_BASE=TRUE)	90D6
85D8 85A6	MXM_LVDS_DDC_DAT	LVDS_EG_DDC_DATA (MAKE_BASE=TRUE)	89A3 90A6
85D8 85A6	MXM_LVDS_DDC_CLK	LVDS_EG_DDC_CLK (MAKE_BASE=TRUE)	89B3 90A8
84C8	CLK_100M_MXM_P	GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE)	9C6 102C3
84C8	CLK_100M_MXM_N	GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE)	9C6 102C3 7C3
84C8	MXM_RESET_L	PEG_RESET_L (MAKE_BASE=TRUE)	9C2 90D4

UNUSED DP INTERFACES

84B5	MXM_DP_C_ML_N<0..3>	TP_MXM_DP_C_ML_N<0..3> (MAKE_BASE=TRUE)
84B5	MXM_DP_C_ML_P<0..3>	TP_MXM_DP_C_ML_P<0..3> (MAKE_BASE=TRUE)
84C5	MXM_DP_C_AUX_N	TP_MXM_DP_C_AUX_N (MAKE_BASE=TRUE)
84C5	MXM_DP_C_AUX_P	TP_MXM_DP_C_AUX_P (MAKE_BASE=TRUE)
84B5	MXM_DP_C_HPD	TP_MXM_DP_C_HPD (MAKE_BASE=TRUE)
84C5	MXM_DP_B_ML_N<0..3>	TP_MXM_DP_B_ML_N<0..3> (MAKE_BASE=TRUE)
84C5	MXM_DP_B_ML_P<0..3>	TP_MXM_DP_B_ML_P<0..3> (MAKE_BASE=TRUE)
84C5	MXM_DP_B_AUX_N	TP_MXM_DP_B_AUX_N (MAKE_BASE=TRUE)
84C5	MXM_DP_B_AUX_P	TP_MXM_DP_B_AUX_P (MAKE_BASE=TRUE)
84C5	MXM_DP_B_HPD	TP_MXM_DP_B_HPD (MAKE_BASE=TRUE)

MXM

EXTERNAL DP CONN

THESE ALIASES ARE TO CONFORM WITH K50/K52 SHARED CONNECTOR PAGE

84C5	MXM_DP_A_ML_N<0>	DP_EG_ML_N<0> (MAKE_BASE=TRUE)	107D2 91D8
84C5	MXM_DP_A_ML_P<0>	DP_EG_ML_P<0> (MAKE_BASE=TRUE)	107D2 91C8
84C5	MXM_DP_A_ML_N<1>	DP_EG_ML_N<1> (MAKE_BASE=TRUE)	107D2 91C8
84C5	MXM_DP_A_ML_P<1>	DP_EG_ML_P<1> (MAKE_BASE=TRUE)	107D2 91C8
84C5	MXM_DP_A_ML_N<2>	DP_EG_ML_N<2> (MAKE_BASE=TRUE)	107D2 91B8
84C5	MXM_DP_A_ML_P<2>	DP_EG_ML_P<2> (MAKE_BASE=TRUE)	107D2 91B7
84C5	MXM_DP_A_ML_N<3>	DP_EG_ML_N<3> (MAKE_BASE=TRUE)	107D2 91C4
84C5	MXM_DP_A_ML_P<3>	DP_EG_ML_P<3> (MAKE_BASE=TRUE)	107D2 91C4
84C5	MXM_DP_A_HPD	DP_EG_HPD (MAKE_BASE=TRUE)	91B4
84D5	MXM_DP_A_AUX_N	DP_EG_AUXCH_N (MAKE_BASE=TRUE)	93C4 107D2
84C5	MXM_DP_A_AUX_P	DP_EG_AUXCH_P (MAKE_BASE=TRUE)	93B4 107D2
84B5	MXM_DP_D_ML_N<0..3>	TP_MXM_DP_D_ML_N<0..3> (MAKE_BASE=TRUE)	
84B5	MXM_DP_D_ML_P<0..3>	TP_MXM_DP_D_ML_P<0..3> (MAKE_BASE=TRUE)	
84B5	MXM_DP_D_AUX_N	TP_MXM_DP_D_AUX_N (MAKE_BASE=TRUE)	
84B5	MXM_DP_D_AUX_P	TP_MXM_DP_D_AUX_P (MAKE_BASE=TRUE)	
84B5	MXM_DP_D_HPD	TP_MXM_DP_D_HPD (MAKE_BASE=TRUE)	

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MXM ALIASES

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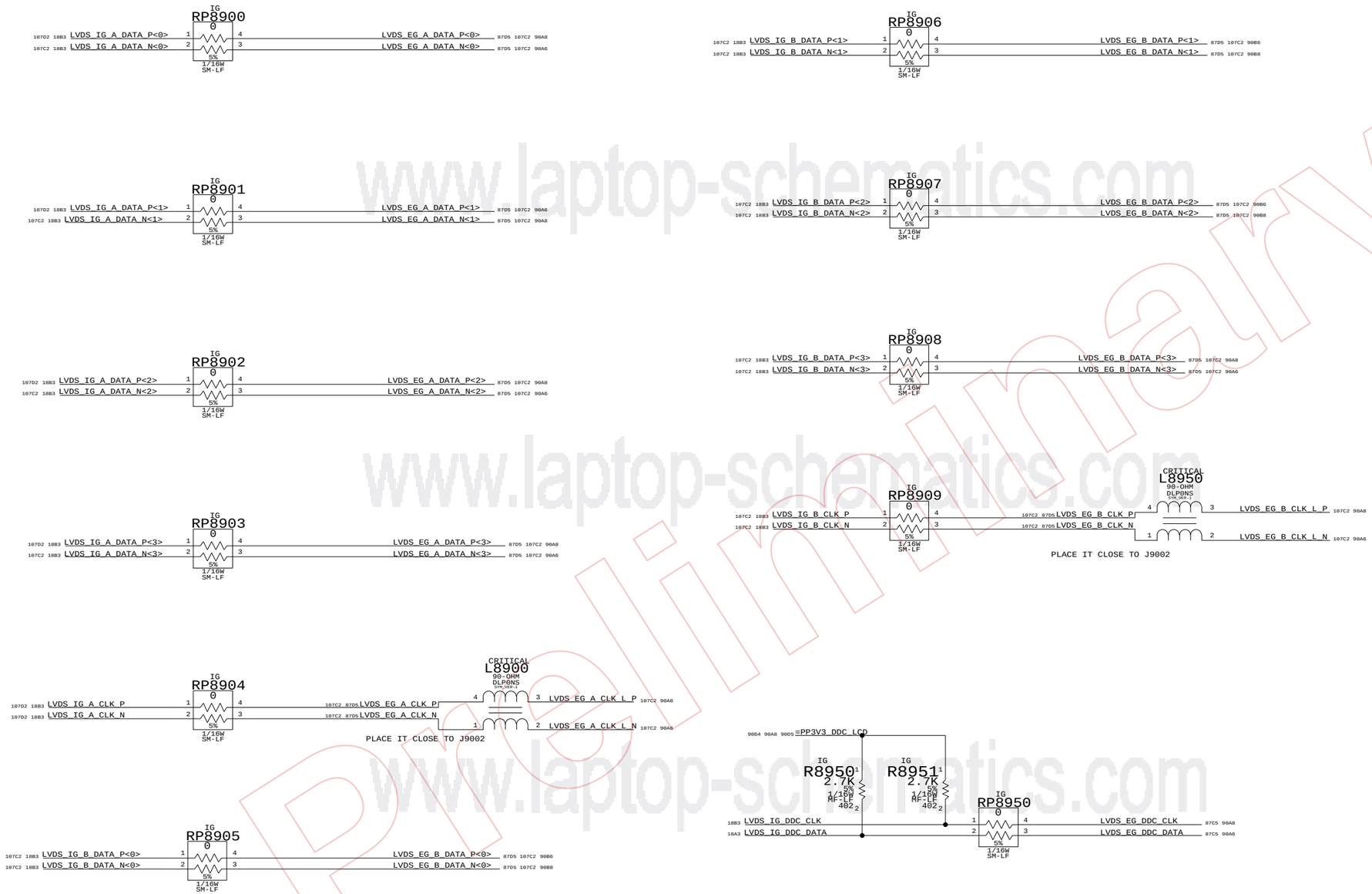

LVDS MUX RESISTORS

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Page Notes

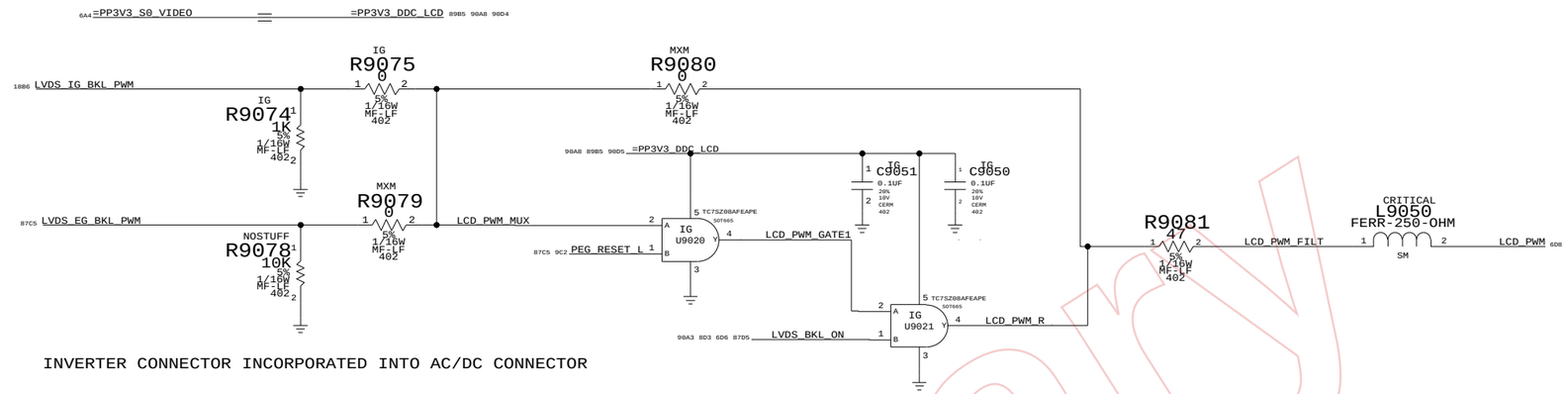
Power aliases required by this page:

- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

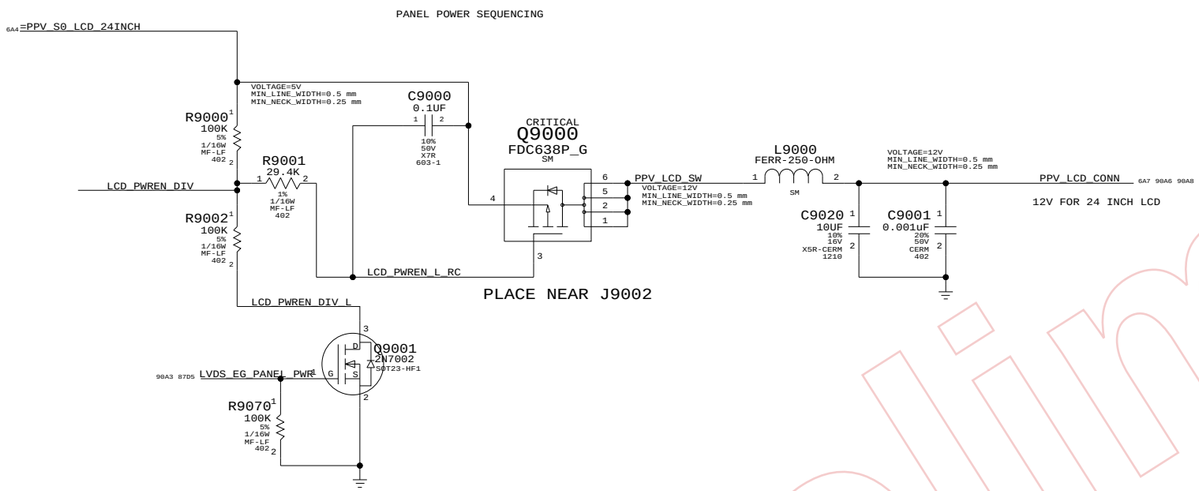
BOM options provided by this page:
IG, MXM

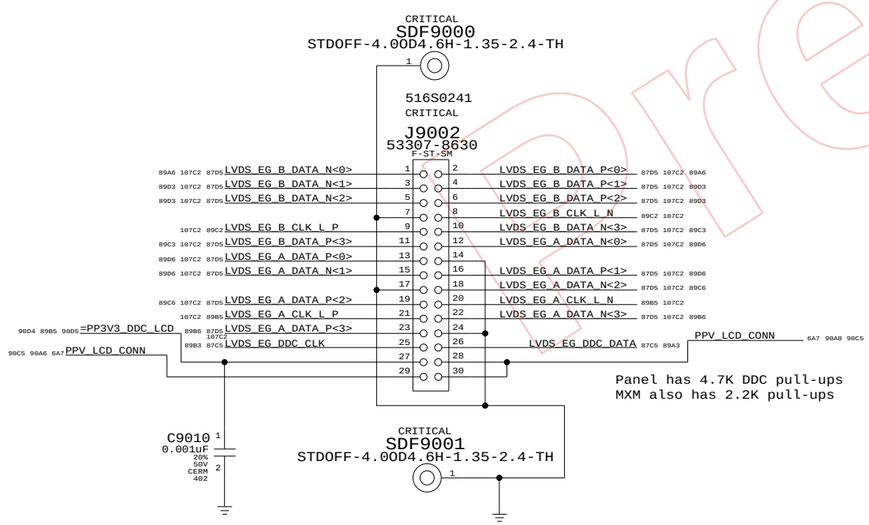
INVERTER INTERFACE



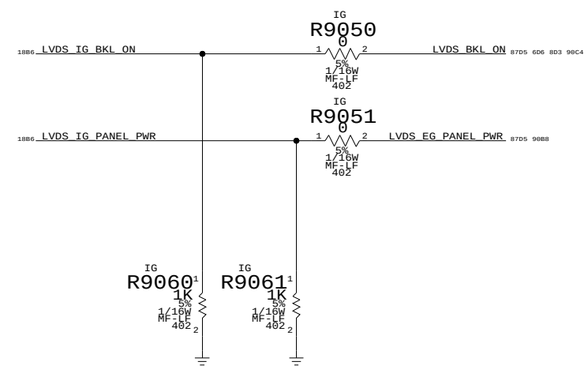
INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

LCD (LVDS) INTERFACE





Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups



INTERNAL DISPLAY CONNS

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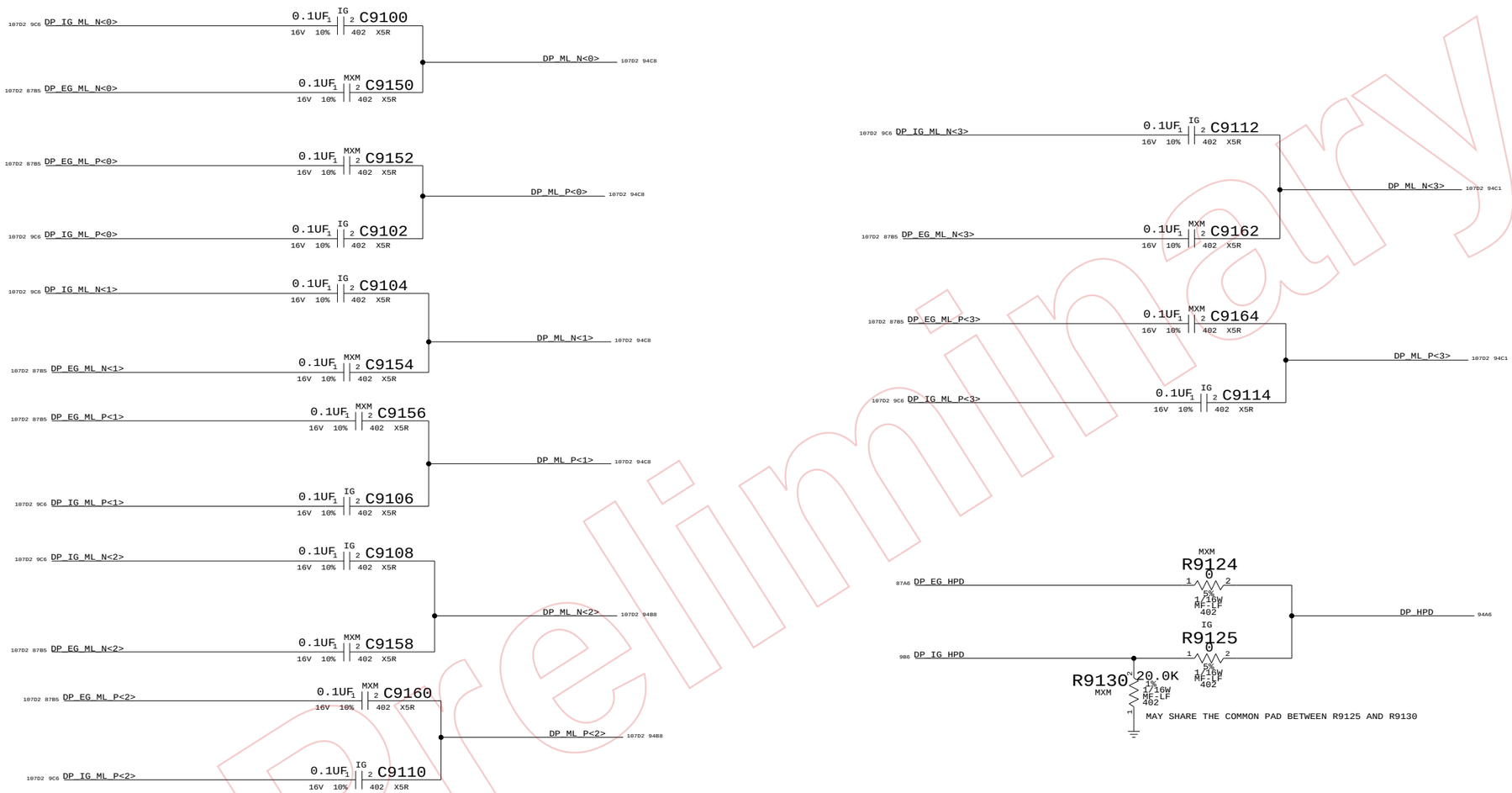

PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

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DP MUX SUPPORT

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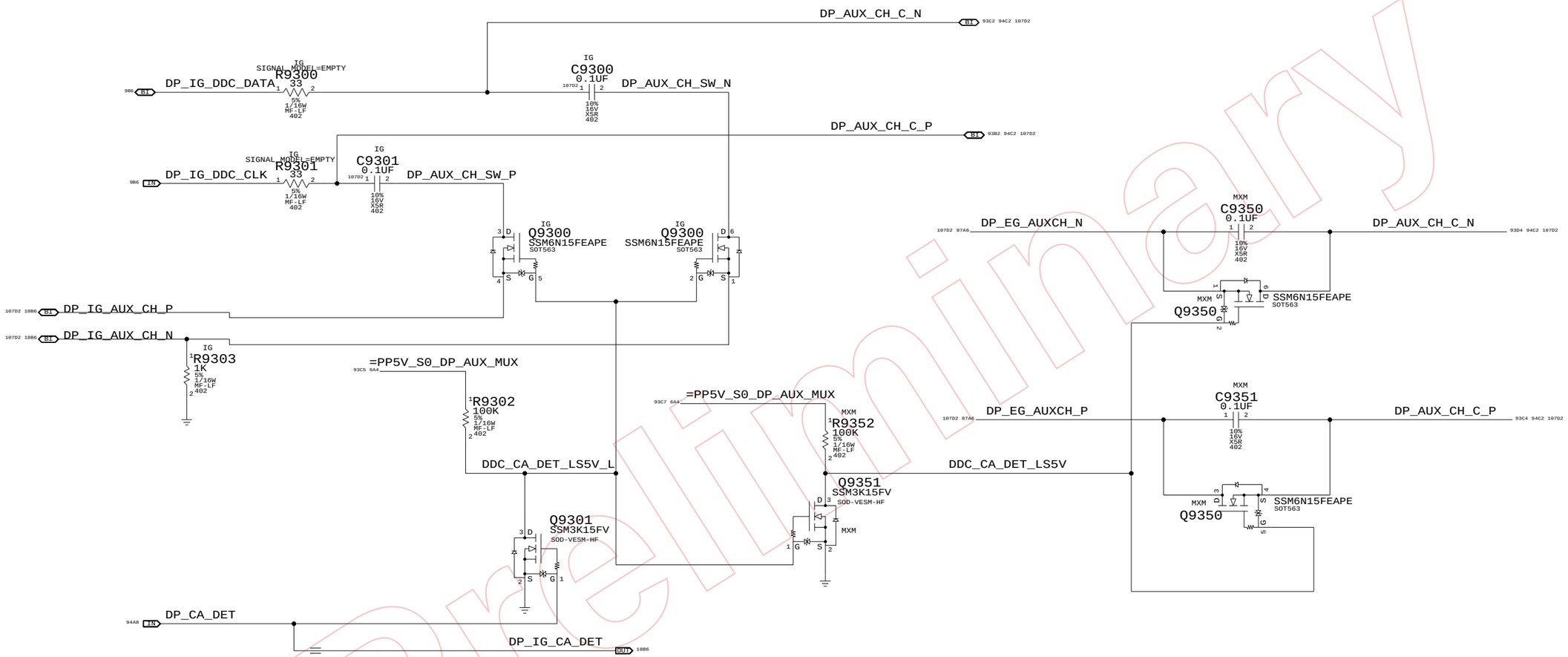

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DISPLAYPORT SUPPORT

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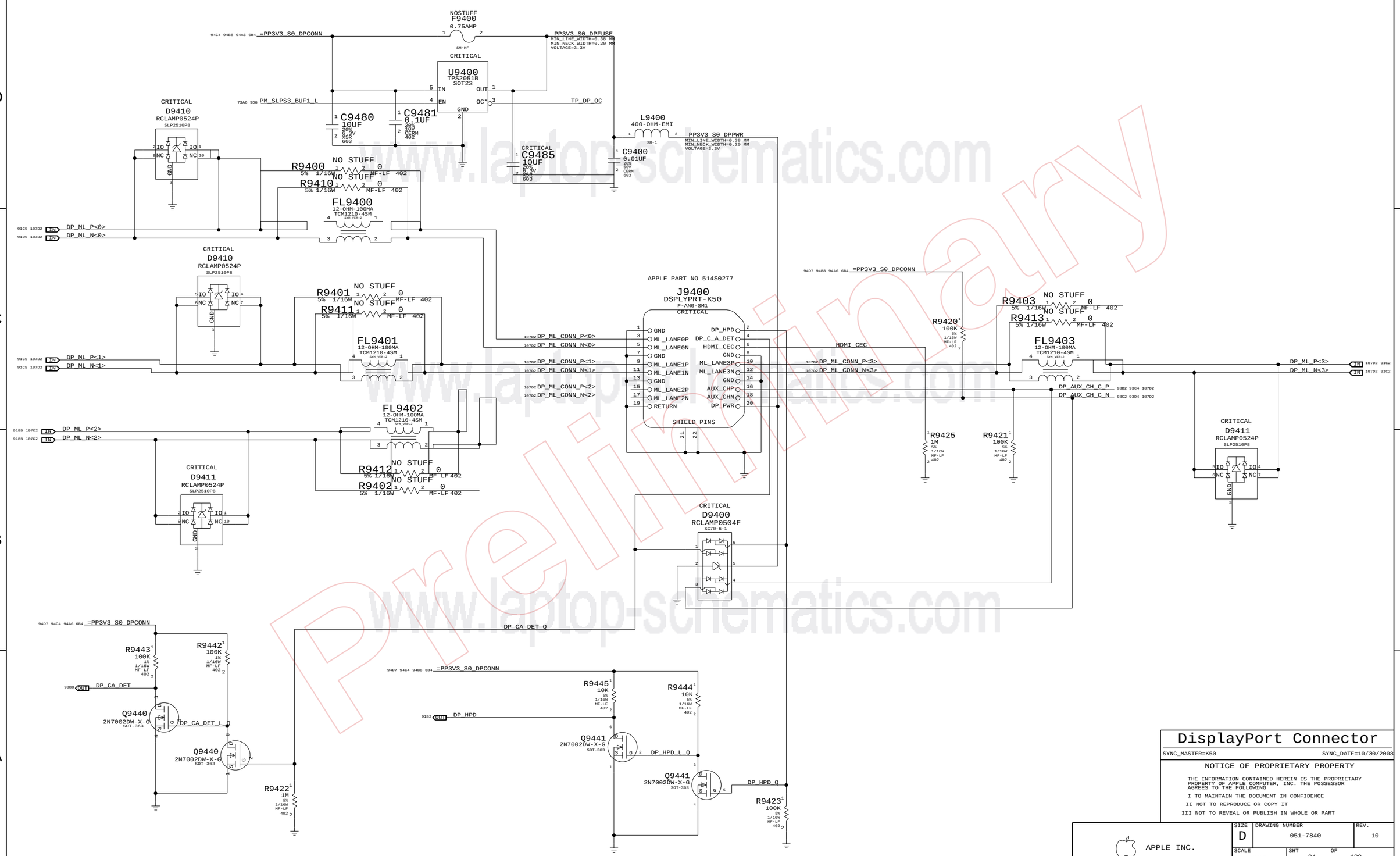

DisplayPort Connector

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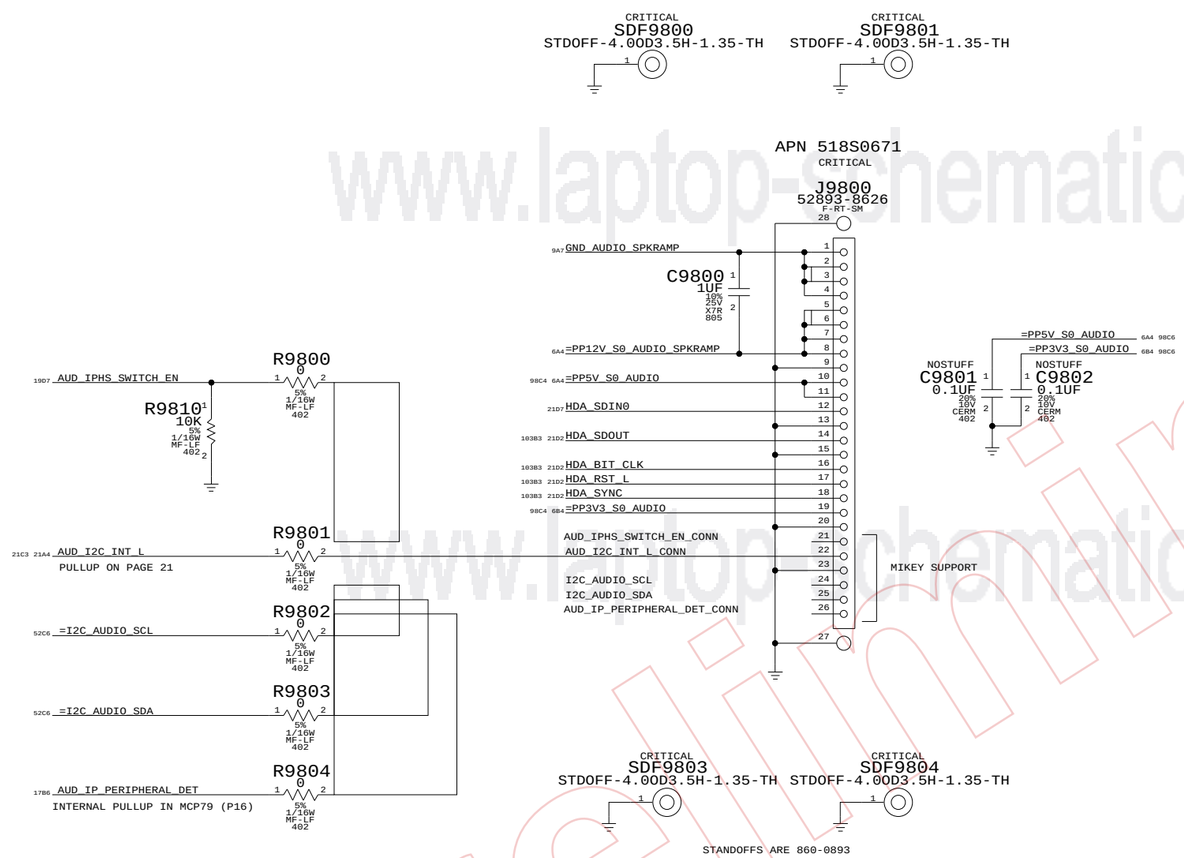

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MLB: AUDIO CONNECTOR

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB_D_L<0>	7D7 7D8 10C4 14D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..1>	10C4 14D3
	FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7D7 7D8 10C4 14D6
	FSB_DSTB0_PP	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7D7 7D8 10C4 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10C4 14D6
	FSB_DATA_GROUP1_PP	FSB_50S	FSB_DATA	FSB_D_L<16>	7D7 7D8 10C4 14D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..17>	10B4 10C4 14C3 14D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10B4 14D6
	FSB_DSTB1_PP	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7D7 7D8 10B4 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10B4 14D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<40..32>	10C2 14C3
	FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB_D_L<41>	7D7 7D8 10C2 14C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..42>	10C2 14B3 14C3
	FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7D7 7D8 10C2 14D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10C2 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7D7 7D8 10C2 14D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<58..48>	10B2 10C2 14B3
	FSB_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB_D_L<59>	7D7 7D8 10B2 14B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..60>	10B2 14B3
	FSB_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7D7 7D8 10B2 14D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10B2 14D6
		FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7D7 7D8 10B2 14D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<5..3>	10D8 14D6
	FSB_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB_A_L<6>	7D7 7D8 10D8 14D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..7>	10D8 14C6 14D6
	FSB_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7C7 7C8 10D8 14B6
	FSB_ADSTB0_PP	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7D7 7D8 10D8 14B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<26..17>	10C8 10D8 14C6
	FSB_ADDR_GROUP1_PP	FSB_50S	FSB_ADDR	FSB_A_L<27>	7D7 7D8 10C8 14C6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..28>	10C8 14C6
	FSB_ADSTB1_PP	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7D7 7D8 10C8 14B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10D6 14B6
	FSB_BREQ0_L_PP	FSB_50S	FSB_1X	FSB_BREQ0_L	7D7 10D6 14B6 23C3
		FSB_50S	FSB_1X	FSB_BREQ1_L	14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_BNR_L	7D7 10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10D6 14B3
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_DBSY_L	7D7 10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10D6 14B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10D6 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_HIT_L	7D7 10D6 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_HITM_L	7D7 10D6 14B6
	FSB_1X_PP	FSB_50S	FSB_1X	FSB_LOCK_L	7D7 10D6 14B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	14A3 23C3 10D6 13C2
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	14A6 10D6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	14B6 10D6
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_A20M_L	7D8 14A3 10C8
	MCP_BSEL	CPU_50S	CPU_AGTL	MCP_BSEL<2..0>	23B6 23C6
	CPU_ASYNC_R	CPU_50S	CPU_8MIL	CPU_FERR_L	10C8 14B7
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_IGNNE_L	7D8 14A3 10C8
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_INIT_L	7D8 14A3 10D6
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_INTR	7D8 14A3 10C8
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_NMI	7D8 14A3 10B8
	CPU_PROCHOT	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10C5 14B6 50B3
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	14A3 7B4 10B2 13C7
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_SMI_L	7C8 14A3 10B8
	CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU_STPCLK_L	7D8 14A3 10C8
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10C6 50B1 14B7
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	14A3 10B2
		CPU_50S	CPU_AGTL	CPU_DPSLP_L	14A3 10B2
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L	14A3 10B2 71C7
		CPU_50S	CPU_AGTL	FSB_DPWR_L	7C7 14A3 10B2
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14A6
	FSB_CLK_CPU_PP	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7C8 14B3 10B6
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7C8 14B3 7B3 10B6
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	14B3 7A4 13C3
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	14B3 7A4 13C3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14A4
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14A4
	CPU_IERR_L	CPU_50S	CPU_AGTL	CPU_IERR_L	10D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21C7 71C8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	71C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	29B2 10B4
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10B3
	XDP_TDI_K50	CPU_50S	CPU_ITP	XDP_TDI	13B3 7A4 10B6 10C6
	XDP_TDO_K50	CPU_50S	CPU_ITP	XDP_TDO	10C6 7A4 10B6 13B3
	XDP_TMS_K50	CPU_50S	CPU_ITP	XDP_TMS	13B3 7A4 10B6 10C6
	XDP_TCK_K50	CPU_50S	CPU_ITP	XDP_TCK	13B6 7A4 10A6 10C6
	XDP_TRST_L_K50	CPU_50S	CPU_ITP	XDP_TRST_L	13B3 7A4 10A6 10C6
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10C6 13C6 7B4
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10C5 13C6 7B4
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	7A4 13C4
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	12C1 71C7
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11B5 71A3
		CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11A5 71A3
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	71A5
		CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	71A5

CPU/FSB Constraints

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7840	10

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Preliminary

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<1..0>	15B5 31C5 31C7
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<1..0>	15B5 31C5 31C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<1..0>	15A5 31D5 31D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<1..0>	15B5 31C5 31C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<1..0>	15B5 31C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15B5 15C5 31C5 31C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15C5 31C5 31C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15C5 31C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15C5 31C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15C5 31C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<6..0>	15B7 31C2 31C4 31D2 31D4
MEM_A_DQ_BYTE0_PP	MEM_40S	MEM_DATA	MEM_A_DQ<7>	7C7 15B7 31C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<13..8>	15B7 31C2 31C4
MEM_A_DQ_BYTE1_PP	MEM_40S	MEM_DATA	MEM_A_DQ<14>	7C7 15B7 31C2
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15>	15B7 31C4
MEM_A_DQ_BYTE2_PP	MEM_40S	MEM_DATA	MEM_A_DQ<16>	7C7 15B7 31B4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..17>	15B7 15C7 31B2 31B4 31C2 31C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<24>	15C7 31C4
MEM_A_DQ_BYTE3_PP	MEM_40S	MEM_DATA	MEM_A_DQ<25>	7C7 15C7 31C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..26>	15C7 31C2 31C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15C7 31B5 31B7 31C5 31C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<46..40>	15C7 15D7 31B5 31B7
MEM_A_DQ_BYTE5_PP	MEM_40S	MEM_DATA	MEM_A_DQ<47>	7C7 15D7 31B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15D7 31B5 31B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<58..56>	15D7 31A7 31B5
MEM_A_DQ_BYTE7_PP	MEM_40S	MEM_DATA	MEM_A_DQ<59>	7C7 15D7 31A7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..60>	15D7 31A5 31A7 31B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15A7 31C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15A7 31C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15B7 31B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15B7 31C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15B7 31B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15B7 31B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15B7 31B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15B7 31A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15D5 31C2
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15D5 31D2
MEM_A_DQS1_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	7C7 15D5 31C4
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15D5 31C4
MEM_A_DQS2_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	7C7 15D5 31B2
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15D5 31C2
MEM_A_DQS3_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	7C7 15D5 31C4
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15D5 31C4
MEM_A_DQS4_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	7B7 15D5 31B7
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15D5 31B7
MEM_A_DQS5_PP	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	7B7 15D5 31B5
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15D5 31B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15D5 31B7
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	7B7 15D5 31B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15D5 31A5
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15D5 31A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<1..0>	15B1 32C5 32C7
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<1..0>	15B1 32C5 32C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<1..0>	15A1 32D5 32D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<1..0>	15B1 32C5 32C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<1..0>	15B1 32C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15B1 15C1 32C5 32C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15C1 32C5 32C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15C1 32C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15C1 32C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15C1 32C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<5..0>	15B3 32C2 32D2 32D4
MEM_B_DQ_BYTE0_PP	MEM_40S	MEM_DATA	MEM_B_DQ<6>	7B7 15B3 32C4
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7>	15B3 32C4
MEM_B_DQ_BYTE1_PP	MEM_40S	MEM_DATA	MEM_B_DQ<8>	7B7 15B3 32C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..9>	15B3 32C2 32C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<22..16>	15B3 15C3 32B2 32B4 32C2 32C4
MEM_B_DQ_BYTE2_PP	MEM_40S	MEM_DATA	MEM_B_DQ<23>	7B7 15C3 32B4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<24>	15C3 32C4
MEM_B_DQ_BYTE3_PP	MEM_40S	MEM_DATA	MEM_B_DQ<25>	7B7 15C3 32C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..26>	15C3 32C2 32C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<37..32>	15C3 32B5 32B7 32C5 32C7
MEM_B_DQ_BYTE4_PP	MEM_40S	MEM_DATA	MEM_B_DQ<38>	7B7 15C3 32B7
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39>	15C3 32B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15C3 15D3 32B5 32B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15D3 32B5 32B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<61..56>	15D3 32A7 32B5 32B7
MEM_B_DQ_BYTE7_PP	MEM_40S	MEM_DATA	MEM_B_DQ<62>	7B7 15D3 32A5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63>	15D3 32A5
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15A3 32C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15A3 32C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15B3 32B4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15B3 32C2
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15B3 32B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15B3 32B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15B3 32B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15B3 32A7

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15D1 32C2
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15D1 32D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15D1 32C4
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15D1 32C4
MEM_B_DQS2_PP	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	7B7 15D1 32B2
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15D1 32C2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15D1 32C4
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	7B7 15D1 32C4
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15D1 32B7
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	7B7 15D1 32B7
MEM_B_DQS5_PP	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	7B7 15D1 32B5
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	7B7 15D1 32B5
MEM_B_DQS6_PP	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	7B7 15D1 32B7
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15D1 32B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15D1 32A5
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	7B7 15D1 32A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16C6

Memory Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9C6 86A7 86B7 86C7 86D7
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9C6 86A7 86B7 86C7 86D7
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	7B7 86A1 86B1 86C1 86D1 9C6
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	7B7 86A1 86B1 86C1 86D1 9C6
PEG_R2D	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	86A5 86B5 86C5 86D5 84A8 84B8
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	86A5 86B5 86C5 86D5 84A8 84B8
PEG_D2R_MXM3	PCIE_90D	PCIE	MXM_PCIE_D2R_P<7..0>	84C8 86A4 86B4 86C4
PEG_D2R_MXM3_PP	PCIE_90D	PCIE	MXM_PCIE_D2R_P<8>	84C8 86C4
PEG_D2R_MXM3	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..9>	84B8 84C8 86C4 86D4
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84B8 84C8 86A4 86B4 86C4 86D4
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34C6
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34C6
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17B3 34B8
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17B3 34C8
PCIE_MINI_D2R_PP	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7C8 34C8 17B6
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7C8 34C8 17B6
	PCIE_90D	PCIE	PCIE_FW_R2D_P	7D6 41C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	7D6 41C3
PCIE_FW_R2D_PP	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17B3 41C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17B3 41C1
PCIE_FW_D2R_PP	PCIE_90D	PCIE	PCIE_FW_D2R_P	7C8 41C1 17B6
	PCIE_90D	PCIE	PCIE_FW_D2R_N	7C8 41C1 17B6
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41C3
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9C6 87C5
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9C6 87C5 7C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17C3 34C6
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17C3 34C6
MCP_PE2_REFCLK_PP	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	7D6 17C3 41C2
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	7D6 17C3 41C2
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18A6 26C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18A6 26C7
MCP_PEX_CLK_COMP	MCP_50S	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6
MCP_IFPAB_RSET	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18A3 26C6
MCP_IFPAB_VPROBE	MCP_50S	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18A3 26C6
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20D6 45D5
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20D6 45D5
	SATA_100D	SATA	SATA_HDD_R2D_P	45D7
	SATA_100D	SATA	SATA_HDD_R2D_N	45D7
SATA_HDD_D2R_PP	SATA_100D	SATA	SATA_HDD_D2R_P	7B8 45C5 20D6
	SATA_100D	SATA	SATA_HDD_D2R_N	7B8 45D5 20D6
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45D7
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45D7
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20D6 45C5
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20D6 45C5
	SATA_100D	SATA	SATA_ODD_R2D_P	45C7
	SATA_100D	SATA	SATA_ODD_R2D_N	45C7
SATA_ODD_D2R_PP	SATA_100D	SATA	SATA_ODD_D2R_P	7B8 45C5 20D6
	SATA_100D	SATA	SATA_ODD_D2R_N	7B8 45C5 20D6
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45C7
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45C7
MCP_SATA_TERMP	MCP_50S	SATA_TERMP	MCP_SATA_TERMP	20A6
PM_SLP_S3_L			PM_SLP_S3_L	21C3 7B4 9D7
PM_SLP_S4_L			PM_SLP_S4_L	21C3 7B4 38D7 49C5 50C3 70D8

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MCP Constraints 1

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	7B3 19D2 19D7
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	7B3 19D2 19D7
PCI_CLK33M_MCP	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19C5
LPC_AD	LPC_55S	LPC	LPC_AD<0>	19B3 49C8 51D5 7D4
LPC_AD_2PP	LPC_55S	LPC	LPC_AD<1>	7B8 7D6 19B3 49C8 51D5 7D4
LPC_AD	LPC_55S	LPC	LPC_AD<3..2>	19B3 49C8 51D4 7D4
	LPC_55S	LPC	LPC_AD_R<3..0>	19B5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19C3 7D4 49C8 51D5
	LPC_55S	LPC	LPC_FRAME_PU	51C2
	LPC_55S	LPC	LPC_FRAME_R_L	19C5 51C1
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19C3 9D4
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19B3 9B4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	9B2 49C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	9B2 7D4 51D4
MCP_SUS_CLK	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R	21B3 9B4
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK	9B2 49C5
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20C4
USB_EXT	USB_90D	USB	USB_EXTA_P	20D3 46A7
	USB_90D	USB	USB_EXTA_N	20D3 46A7
	USB_90D	USB	USB_PORT0_P	46A5
	USB_90D	USB	USB_PORT0_N	46A5
USB_EXT	USB_90D	USB	USB_EXTB_P	20C3 46B6
	USB_90D	USB	USB_EXTB_N	20C3 46B6
	USB_90D	USB	USB_PORT1_P	46B5
	USB_90D	USB	USB_PORT1_N	46B5
USB_EXT	USB_90D	USB	USB_EXTC_P	20C3 46B3
	USB_90D	USB	USB_EXTC_N	20C3 46B3
	USB_90D	USB	USB_PORT2_P	46B2
	USB_90D	USB	USB_PORT2_N	46B2
USB_EXT_MUXED	USB_90D	USB	USB_EXTD_P	20D3 46D5
	USB_90D	USB	USB_EXTD_N	20D3 46D5
	USB_90D	USB	USB_D_MUXED_P	46D4
	USB_90D	USB	USB_D_MUXED_N	46D4
	USB_90D	USB	USB_PORT3_P	46D3
	USB_90D	USB	USB_PORT3_N	46D3
USB_MINI	USB_90D	USB	USB_MINI_P	20D3 34B3
	USB_90D	USB	USB_MINI_N	20D3 34B3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7B8 20D3 47B7
	USB_90D	USB	USB_CAMERA_N	7B8 20D3 47B7
	USB_90D	USB	USB_CAMERA_L_P	47B6
	USB_90D	USB	USB_CAMERA_L_N	47B6
USB_BT_PP	USB_90D	USB	USB_BT_P	7B8 20D3 47D4
	USB_90D	USB	USB_BT_N	7B8 20C3 47D4
USB_IR	USB_90D	USB	USB_IR_P	20D3 47B4
	USB_90D	USB	USB_IR_N	20D3 47B4
USB_IR	USB_90D	USB	USB_IR_L_P	47B3
	USB_90D	USB	USB_IR_L_N	47B3
SPI_CLK	MCP_50S	SPI	SPI_CLK_R	7B8 21B3 51A6 61C6
	MCP_50S	SPI	SPI_CLK	61C5
SPI_MOSI	MCP_50S	SPI	SPI_MOSI_R	21B3 51A6 61C2
	MCP_50S	SPI	SPI_MOSI	61C4
SPI_MISO	MCP_50S	SPI	SPI_MISO	7B8 51A6 61B2 21B3
	MCP_50S	SPI	SPI_MISO_R	61B4
SPI_CS0	MCP_50S	SPI	SPI_CS0_R_L	21B3 51C6
	MCP_50S	SPI	SPI_CS0_L	51C7
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21D2 98C6
	HDA_55S	HDA	HDA_BIT_CLK_R	21D4 21A7
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	21D2 98C6
	HDA_55S	HDA	HDA_RST_R_L	21D4 21A7
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21D2 98C6
	HDA_55S	HDA	HDA_SDOUT_R	21D4 21A7
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21D2 98C6
	HDA_55S	HDA	HDA_SYNC_R	21D4 21A7

MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18C3 38B3
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	38B2 37B6
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18C3 37B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18D3 37B6
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	37C1 18D6
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	37C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	37C1 18D6
	ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	37C4
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	37C1 18D6
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	37C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	37B1 18D6
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	37B4
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18D3 37C7
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18D3 37C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18D3 37C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18D3 37B6
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	37B3 39C5 39C6 39C7 39C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	37B3 39C5 39C6 39C7 39D8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	39C1 39A4 39A5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	39C1 39D1 39A4 39A5

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Ethernet Constraints

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FIT:

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	42C2 43B5
	FW_110D	FW_TP	FW_PORT0_TPA_N	42C2 43C5
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	42C2 43C5
	FW_110D	FW_TP	FW_PORT0_TPB_N	42C2 43C5

PORT 1 & 2 NOT USED

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FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	52D2
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	52D2
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	52C5
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	52C5
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	52D5
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	52D5
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	52C2
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	106D3 52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	106D3 52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	106D3 52C2
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	106D3 52C2
	SMB_55S	SMB	SMBUS_MCP_0_CLK	13B6 21C3 7A4 52D8
	SMB_55S	SMB	SMBUS_MCP_0_DATA	13B6 21C3 7A4 52D8

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SMC Constraints

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>	87B5 91B7 91C4 91C8
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9C6 91B7 91B8 91C4 91C8
	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>	87B5 91B8 91C4 91C8 91D8
	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9C6 91B8 91C8 91D4 91D8
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	91B5 91C2 91C5 94B8 94C1 94C8
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	91B5 91C2 91C5 91D5 94B8 94C1 94C8
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	94C4 94C5
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	94C4 94C5
DP_IG_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18B6 93C8
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18B6 93C8
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	93C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	93D5
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	93B2 93C4 94C2
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	93C2 93D4 94C2
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUXCH_P	87A6 93B4
	DP_100D	DISPLAYPORT	DP_EG_AUXCH_N	87A6 93C4
LVDS_A_CLK_MXM3	LVDS_100D	GND	LVDS_IG_A_CLK_P	18B3 89B8
	LVDS_100D	GND	LVDS_IG_A_CLK_N	18B3 89B8
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3..0>	18B3 89B8 89C8 89D8
	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3..0>	18B3 89B8 89C8 89D8
LVDS_B_CLK_MXM3	LVDS_100D	GND	LVDS_IG_B_CLK_P	18B3 89C5
	LVDS_100D	GND	LVDS_IG_B_CLK_N	18B3 89C5
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3..0>	18B3 89A8 89C5 89D5
	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3..0>	18B3 89A8 89C5 89D5
LVDS_A_CLK_MXM3	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	87D5 89B6
	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	87D5 89B6
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<3..0>	87D5 89B6 89C6 89D6 90A6 90A8
	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<3..0>	87D5 89B6 89C6 89D6 90A6 90A8
LVDS_B_CLK_MXM3	LVDS_100D	LVDS	LVDS_EG_B_CLK_P	87D5 89C3
	LVDS_100D	LVDS	LVDS_EG_B_CLK_N	87D5 89C3
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<3..0>	87D5 89A6 89C3 89D3 90A8 90B6
	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<3..0>	87D5 89A6 89C3 89D3 90A6 90B8
	LVDS_100D	LVDS	LVDS_EG_A_CLK_L_P	89B5 90A8
	LVDS_100D	LVDS	LVDS_EG_A_CLK_L_N	89B5 90A6
	LVDS_100D	LVDS	LVDS_EG_B_CLK_L_P	89C2 90A8
	LVDS_100D	LVDS	LVDS_EG_B_CLK_L_N	89C2 90A6

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	600 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6D3 31A5 31D7
		PPDDR_MEM	=PP1V5_S3_MEM_B	6D3 32A5 32D7
		SWITCHNODE	IMVP6_PHASE1	71D4 71A6
		SWITCHNODE	IMVP6_PHASE2	71C4 71A4
		SWITCHNODE	IMVP6_PHASE3	72C6 72A7
		SWITCHNODE	1V8_SW	88C5
		SWITCHNODE	1V05S5_SW	79C5
		SWITCHNODE	P1V05S0_PHASE	76C6
		SWITCHNODE	3V3S5_SW	76C3
		SWITCHNODE	5VS3_SW	73C5
		SWITCHNODE	MCPCORES0_PHASE	74C5
THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55A8 55D6 55D8
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55A8 55D6 55D8
THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55A8 55C6 55C8
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55A8 55C6 55C8
THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P	10C6 55D4
	THERM_DIFF	THERMAL	CPU_THERMD_N	10C6 55D4
THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55A8 55B6 55B8
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55A8 55B6 55B8
THERM_DIFF	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21C3 55C4
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21C3 55C4
THERM_DIFF	THERM_DIFF	THERMAL	MCPTHMSNS_D2_P	55B3
	THERM_DIFF	THERMAL	MCPTHMSNS_D2_N	55B3
THERM_DIFF	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53C4
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53C4
THERM_DIFF	THERM_DIFF	THERMAL	SENSE_12V_S0_P	53B3 53B4
	THERM_DIFF	THERMAL	SENSE_12V_S0_N	53B3 53B4
THERM_DIFF	THERM_DIFF	THERMAL	SENSE_12V_S5_P	53B3 53C4
	THERM_DIFF	THERMAL	SENSE_12V_S5_N	53B3 53C4
THERM_DIFF	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54D6
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54D6
THERM_DIFF	THERM_DIFF	THERMAL	SNS_LCD_P	55C7
	THERM_DIFF	THERMAL	SNS_LCD_N	55C7
THERM_DIFF	THERM_DIFF	THERMAL	SNS_ODD_P	55D7
	THERM_DIFF	THERMAL	SNS_ODD_N	55D7
THERM_DIFF	THERM_DIFF	THERMAL	SNS_CPU_H_P	55B7
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55B7
THERM_DIFF	THERM_DIFF	THERMAL	SNS_HDD_P	55D6
	THERM_DIFF	THERMAL	SNS_HDD_N	55D6
THERM_DIFF	THERM_DIFF	THERMAL	HDD_OOB_TEMP_FILT	55D6
THERM_DIFF	THERM_DIFF	THERMAL	SNS_AMB_P	55C6
	THERM_DIFF	THERMAL	SNS_AMB_N	55C6
THERM_DIFF	THERM_DIFF	THERMAL	SNS_MXM_P	55B6
	THERM_DIFF	THERMAL	SNS_MXM_N	55B6
THERM_DIFF	THERM_DIFF	THERMAL	MCPTHMSNS_FILT_P	55B4
	THERM_DIFF	THERMAL	MCPTHMSNS_FILT_N	55B4

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K50/K51 SPECIFIC CONSTRAINTS

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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.345 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.19 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.125 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.121 MM	0.085 MM	=STANDARD	0.18 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.085 MM	=STANDARD	0.180 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	0.3 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
1:1_DIFFPAIR	TOP,BOTTOM	Y	=STANDARD	=STANDARD	=STANDARD	0.125 MM	0.085 MM

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM
MCP_HDA_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

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K50/K51 RULE DEFINITIONS

SYNC_MASTER=K50 SYNC_DATE=10/30/2008

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